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A Deep Study of Resistance Switching Phenomena in TaO_x ReRAM Cells: System-Theoretic Dynamic Route Map Analysis and Experimental Verification

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The multidisciplinary field of memristors calls for the necessity for theoretically-inclined researchers and experimenters to join forces, merging complementary expertise and technical know-how, to develop and implement rigorous and systematic techniques to design variability-aware memristor-based circuits and systems. The availability of a predictive physics-based model for a memristor is a necessary requirement before commencing these investigations. An interesting dynamic phenomenon, occurring ubiquitously in non-volatile memristors, is fading memory. The latter may be defined as the appearance of a unique steady-state behavior, irrespective of the choice of the initial condition from an admissible range of values, for each stimulus from a certain family, for example, the DC or the purely-AC periodic input class. This paper first provides experimental evidence for the emergence of fading memory effects in the response of a TaO_x redox-based random access memory cell to inputs from both of these classes. Leveraging the predictive capability of a physics-based device model, called JART VCM v1, a thorough system-theoretic analysis, revolving around the Dynamic Route Map graphic tool, is presented. This analysis allows to gain a better understanding of the mechanisms, underlying the emergence of history erase effects, and to identify the main factors, that modulate this nonlinear phenomenon, toward future potential applications.

1. Introduction

The predictive power of Moore's law[1] is about to fade away, as CMOS technology scaling approaches atomic boundaries. Moreover, as the technology minimum feature size is progressively reduced toward the lowest physically-possible limit, the resulting increase in leakage currents poses serious issues in two significant directions. First, it results in serious heat issues, which may jeopardize the life-time of circuits, and create dangerous positive feedback effects in the thermally-activated physical mechanisms, underlying the operating principles of certain devices. Concurrently, it leads to an inevitable upsurge in power consumption across a CMOS chip, which sheds shadows on the reliability of Dennard's law,[2] and prevents further increases in the clock frequency. Taking also into account the extremely-high costs associated with the production of cutting-edge sub-10 nm chips, semiconductor manufacturers are questioning whether keeping the aggressive transistor downscaling rate, dictated by Moore's law, is still profitable.[3] An additional aspect, which limits the maximum information management rate, is related to the classical von Neumann architecture of state-of-the-art computers, in which the physical separation between central processing unit and data storage system causes inevitable delays in the accomplishment of memory and computing tasks. Besides the proposal of clever ideas to resolve some of these open issues, for example, exploiting the third vertical direction to increase the transistor count on the available chip area, and developing multi-core computing machines with distributed memory to increase the data processing rate, device engineers are devoting considerable efforts in the search for special materials, allowing to develop

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novel devices, which, featuring multiple functionalities within a single nanoscale physical volume, would allow to boost the performance of integrated circuits beyond the technology, heat, energy, and architecture walls, in the years to come.[4]

In this regard, one of the most promising class of devices are the memory-resistors, for short memristors,[5,6] which may be essentially defined as nonlinear resistors endowed with a state-dependent Ohm law,[7,8] similarly as the constitutive units of biological neural networks, that is, synapses and neuronal ion channels, which explains why they may pave the way toward the design of brain-like computing machines in the near future.[9–11] In particular, depending upon fabrication process, constitutive material, and operating conditions, memristor physical realizations, often referred to as resistance switching devices in the material engineering community,[12] may either be non-volatile or volatile.[13] In the first (latter) case, switching the power off, each device of this kind freezes instantaneously at one of an analogue continuum of memory states[14] (settles down, after some transient phase, on one and only one memory state, irrespective of the initial condition[15]). Besides realizing an innovative resistance–based data storage concept, and reproducing synaptic plasticity,[16] non-volatile memristors may allow to implement in-memory computing paradigms.[17,18] Volatile memristors are typically employed as selector devices[19] to regulate the current flow in crossbar arrays of non-volatile memristors, but they may be also utilized to implement spike-based computing paradigms,[10] or to develop biologically-plausible electronic implementations of neurons,[20–22] if, similarly as sodium and potassium ion channels in axon membranes,[23] exhibit the capability to amplify the small-signal upon suitable polarization,[15,24,25] a property which is referred to as local activity.[26]

The research work, presented in this manuscript, aims to highlight the pivotal role that nonlinear system theory may assume in deepening the understanding of intrinsically-nonlinear devices[27] toward a systematic analysis and design of circuits based upon them.[28] Back in 2016 TU Dresden and Hewlett Packard (HP) Labs announced the discovery of a very interesting input-induced dynamic phenomenon, referred to as fading memory[29] or history erase effect,[30] in a tantalum oxide-based non-volatile nano-device. Due to the application of a purely-AC periodic voltage across the memristor, its current was found to feature, asymptotically, one and only one oscillatory behavior, irrespective of the memory content preliminarily programmed into the device resistance. Further investigations revealed that history erase effects appear in the non-volatile memory cell from HP Labs also under a constant voltage stimulus of either polarity, resulting in a unique steady-state level for the current through its physical stack, irrespective of the device resistance prior to the DC stress test.

While input-induced memory loss effects were later observed in various other non-volatile memristors,[31,32] this manuscript conducts a deep study, combining experimental work and nonlinear system-theoretic methods, to gain a deep insight into the origin of this nonlinear phenomenon, and to determine the key parameters enabling its modulation in view of future potential applications. The object of the investigations is an illustrative example of a filamentary valence change memory (VCM) cell, specifically a tantalum oxide redox-based random access memory (ReRAM) device fabricated at Peter Grünberg Institut (PGI-7), Forschungszentrum Jülich GmbH. As for all filamentary VCM cells, the modulation of the resistance of the physical stack under focus is enabled by the restoration and rupture of a tiny conductive filament region, featuring a high concentration of oxygen vacancies, which occur under complementary polarities of the voltage let to drop across the device terminals. In this paper, experimental evidence for the fading memory behavior of the ReRAM cell under either DC or purely-AC periodic excitation is first provided. Furthermore, a powerful system-theoretic tool, called *dynamic route map* (DRM),[33] is applied to an accurate physics-based first-order model of the non-volatile memory cell, allowing for a deeper understanding of the unique device behavior. Moreover, a novel graphic tool, called *current DRM* (C-DRM), is proposed, so as to enable a similar circuit-theoretic analysis based on experimentally available data.

2. Experimental Results on DC Stress Tests

In order to enable the investigation of the typical resistance switching characteristics of VCM cells, an exemplary ReRAM device, composed of a platinum (Pt) / tantalum oxide (TaO_x)/ tantalum (Ta)/Pt physical stack (refer to **Figure 1**a), was preliminarily fabricated, and electrically characterized in house.

Figure 1b shows also a top-view scanning electron microscope (SEM) image of a micro-crossbar VCM cell, featuring a junction area of $3 \times 3\ \mu m^2$, and its TEM cross-section, revealing the thickness of each layer of the device stack. Details on the device fabrication are reported in Section 7.

The electrical characterization of the crosspoint devices is performed at room temperature using a custom setup[34] designed in house. Figure 1b shows 50 cycles of a current i_m–voltage v_m characteristic of the Pt/TaO_x/Ta/Pt ReRAM device, as acquired through the application of a slowly-varying asymmetric AC periodic triangular voltage stimulus with a frequency of 2 kHz, a minimum value of –0.7 V, and a maximum value of +1.6 V to the bottom electrode, with the top electrode grounded. Over each cycle, the VCM cell undergoes a SET (RESET) transition over the negative (positive) half cycle of the input waveform. Stimulating the bipolar ReRAM device through a high-frequency asymmetric AC periodic voltage pulse train, it is found to exhibit a very reliable resistance switching behavior, undergoing consecutive SET and RESET transitions for as many as 10^6 cycles.[35]

Focusing again on the *I–V* characteristic in Figure 1b, it becomes clear that, over the SET process, the resistance of the device initially undergoes a rather abrupt thermally-activated decrease, while, later on, as the current attains higher values, the increase in the voltage across the internal series resistance limits its further reduction.[36] Similarly, over the RESET process, which starts at high current levels, the device resistance undergoes initially a noticeable thermally-activated increase, until its further growth is counteracted by the negative feedback mechanism that naturally comes into play as the device draws less current.[36] Importantly, the saturation phenomena, emerging in the second phase of each of the SET and RESET resistance switching transitions, are responsible for the memory loss induced in the device by DC inputs, which clearly reveals the fundamental role of the internal series resistance on the emergence of the *fading memory* phenomenon. Section S1, Supporting Information, provides more details on the system-theoretic concept of fading memory. Figure 1c(d) provides evidence for the fading memory of

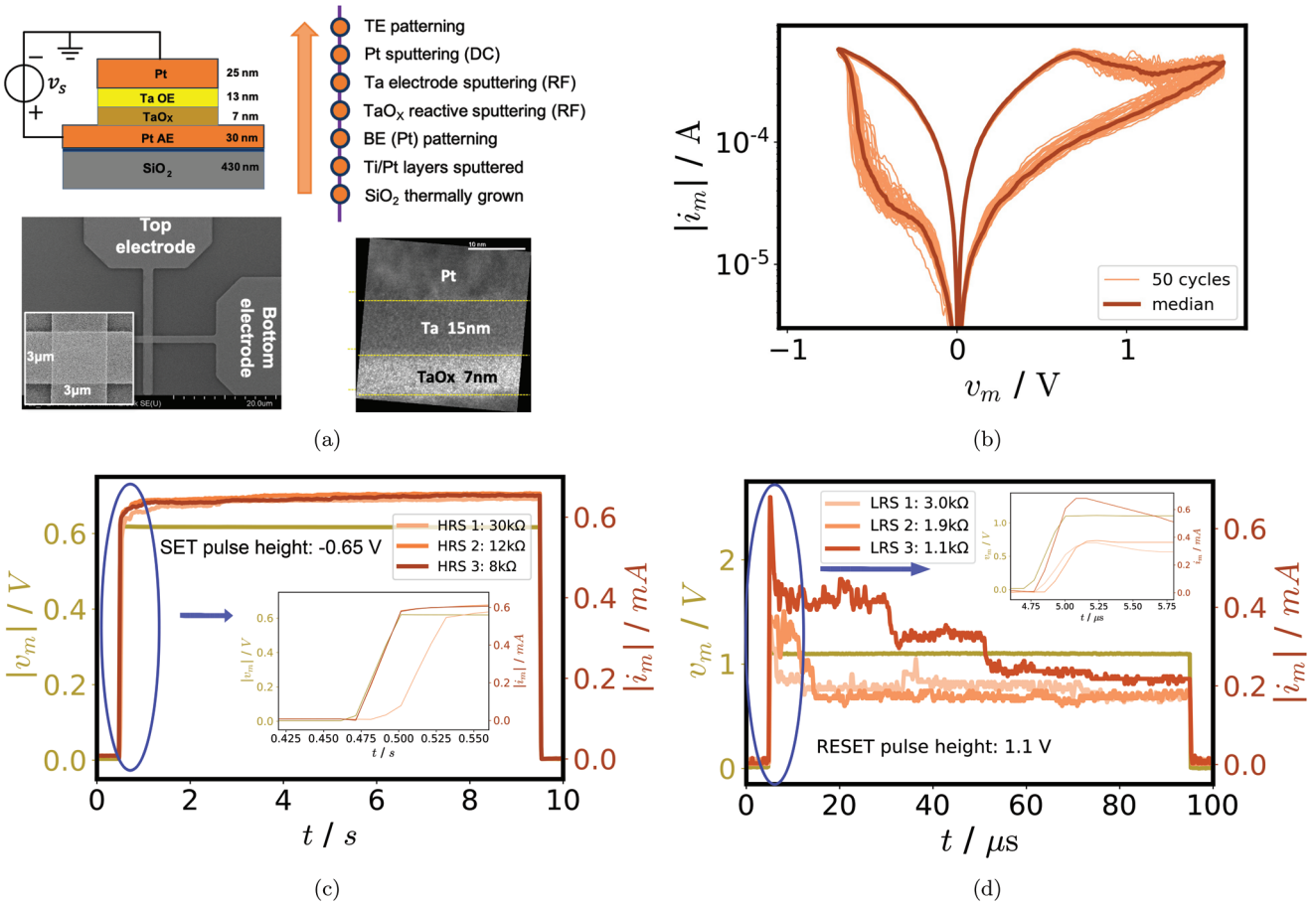


Figure 1. a) Schematic diagram and fabrication process flow of a Pt(25 nm)/Ta(15 nm)/TaO_x(7nm)/Pt(30 nm) ReRAM device, including a top-view SEM image of a 3×3 μm^2 VCM cell, and its TEM cross-section providing clear evidence for the thickness of each layer in the physical stack. b) Current i_m–voltage v_m characteristic of a Pt/Ta/TaO_x/Pt VCM cell for 50 switching cycles of a quasi-static asymmetric triangular voltage stimulus cycling periodically at a frequency of 2 kHz and featuring minimum and maximum values −0.7 V and +1.6 V, respectively (light orange). The median cycle is shown in dark orange. The application of the voltage stimulus to the bottom electrode, with the top electrode grounded, explains why, over each 0.5 ms-long cycle, the device undergoes a SET (RESET) resistance switching transition in the negative (positive) half of the input waveform. c,d) Experimental evidence for the memory loss, which DC inputs induce in the device. Transients in the device current under the application of a given set voltage pulse for three different initial conditions established preliminarily through distinct reset operations (c). Transients in the device current under the application of a given reset voltage pulse for three different initial conditions established preliminarily through distinct set operations (d). The insets in (c) and (d) are close-up views across the pulse rise time interval, indicated through blue ellipses in the original plots. A high resistance state (HRS) is preliminarily programmed into the device through the selection of a particular value for the peak, called *reset-stop voltage*,[12] of a purely-positive slowly-and-stepwise-varying triangular pulse signal applied across the physical structure. In order to program a low resistance state (LRS) into the device, prior to the DC stress reset test, the current response of the physical stack to a purely-negative slowly-and-stepwise-varying triangular pulse signal is hard limited by specifying a particular *compliance level* in the measurement setup.

the ReRAM device under a negative (positive) DC input voltage. Preliminarily, the device was programmed into one of three low (high) resistance states, as indicated in the legend. A negative (positive) voltage pulse, featuring a height of −0.65 V (1.1 V), a width of 9.007 s (90.07 μs), and a rise and fall time of 40.1 ms (401 ns), was then found to induce a progressive memory loss, which results in the appearance of a unique steady state for the current flowing through the physical stack. With reference to the SET transition of Figure 1c, the dynamics of the device are first accelerated by the positive feedback induced by Joule heating effects, but are then slowed down and limited by the inherent series resistance. Consequently, the device current attains a unique saturation plateau, for each of the three initial conditions (HRS stands for high resistance state), before returning to zero in all cases, when the power is switched off. This experiment shows how DC fading memory coexists with non-volatility in the VCM cell. The initial condition affects only the onset of the VCM device response, which commences with some small delay after (commences directly after) the pulse stimulus begins its ascent in the most resistive case (in the two least resistive cases). Looking now at the experimental results from Figure 1d, the pulse rise causes an initial upsurge in the device current. Then, when the RESET transition commences, the device current first experiences a strong decrease. This is induced by the positive feedback mechanisms, setting in as, by nonlinear voltage division, the fraction of the total ReRAM cell voltage, falling across the core memristor, progressively and inevitably dominates more and more over the remainder, dropping across the internal series resistance. Later, when most of the

positive bias voltage stimulus falls across the core memristor, the low device current levels determine a thermal deactivation of the RESET switching dynamics. In fact, due to the negative feedback effects, associated with the ongoing cooling of the internal filament, in this second phase the device current is found to decrease more gradually. Importantly, the current, flowing through the device stack, is found to tend toward a common asymptotic level, for each of the three initial conditions (LRS stands for low resistance state). Finally, in all scenarios, when the input is removed, the device current drops to zero. This result reveals, once again, the coexistence between fading memory, as induced by DC stimulation, and non-volatility, appearing when the power is switched off, in the ReRAM device.

3. System-Theoretic Insights into the Device Resistance Switching Transitions under DC Stress

The next section reports the main equations of the physics-based mathematical model,[37–39] which reproduces accurately the response of our TaO_x ReRAM device to any input of interest and for all admissible initial conditions. More details on the VCM cell mathematical description are given in Section S2, Supporting Information, which includes also the complete list of model parameters. A deep system-theoretic analysis of the DC SET and RESET transitions of the VCM cell is then conducted on the basis of this model.

3.1. JART VCM v1 ReRAM Model

Figure 2a depicts the equivalent circuit-theoretic description of the JART VCM v1 model. Its consists of the series combination between a number of resistances identifiable along the longitudinal extension of the ReRAM device. With the physical stack rotated by –90° relative to its view in Figure 1a, the Ta-based top (Pt-based bottom) electrode, which is referred to as ohmic (active) electrode, or OE (AE) for short, throughout the manuscript, is adjacent to the left (right) end of the TaO_x-based oxide layer. Here v_m, and i_m, respectively denote the voltage falling across and the current flowing through the device, which, as shown in Figure 2b, is symbolized as a memristor[5] in circuit and system theory. The physical origin for the SET and RESET switching processes is known as VCM mechanism.[40] It is associated with the motion of ionic defects—in particular, the positively-charged oxygen vacancies—from the OE/oxide interface toward the oxide/AE interface (from the oxide/AE interface toward the OE/oxide interface) as a negative (positive)-valued voltage v_m is let fall across the device. In the first (latter) case, this results in the formation (dissolution) of a conductive filament, bridging (opening up) a gap between the two electrodes, at the oxide/AE interface. As a basic assumption of the JART VCM v1 model, the oxygen vacancy-rich conductive filament, which is first created within the oxide film through an electro-forming step, is composed of two main resistive regions. One of them, called *plug*, features a large number of ionic defects, and, as a result, acts as an oxygen vacancy reservoir for the other less conductive region, named *disc*. The motion of ionic defects toward the AE (OE) under a negative (positive) voltage stimulus v_s across the micro-scale device determines an increase (decrease) in the disc oxygen vacancy concentration N_{disc}, which defines the *VCM cell state*. Importantly, N_{disc} is constrained to lie at all times within a closed set, defined as $\mathcal{D} \triangleq [N_{disc,off}, N_{disc,on}]$, where the lower (upper) bound is associated to the device highest (lowest) possible resistance state. The ordinary differential equation (ODE), governing the time evolution of the disc oxygen vacancy concentration, is then expressed by

$$\frac{dN_{disc}}{dt} = f(N_{disc}, v_m, i_m) = -\frac{i_{ion}}{z_{V_O} \times e \times A \times l_{disc}} \tag{1}$$

in which i_{ion} stands for the ion-hopping current, related through complex implicit equations to memristor state N_{disc}, voltage v_m, and current i_m, as established by the Mott– Gurney law, while the

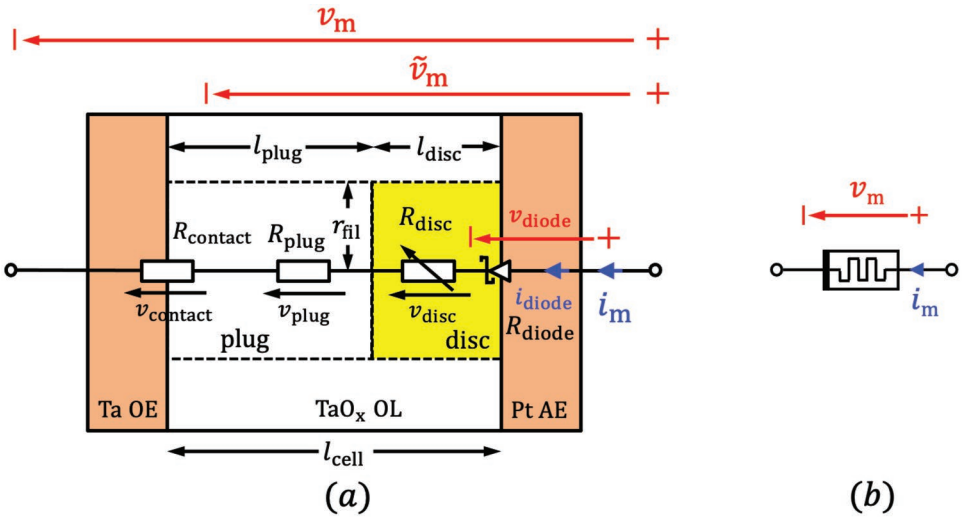


Figure 2. a) Circuit-theoretic model and b) symbol of the TaO_x-based VCM cell. The memristor state is defined as the oxygen vacancy concentration N_{disc} in the disc region. The device voltage, and current are indicated as v_m, and i_m, respectively. The VCM cell may be interpreted as a one resistor-one memristor two-terminal device. The role of the resistive element is assumed by the contact resistance $R_{contact}$, which forms naturally at the OE/oxide interface. OE, AE, and OL, respectively stands for ohmic electrode, active electrode, and oxide layer.

other symbols are constant parameters. Given that the OE/oxide interface operates purely as a linear resistor, it is the electric field-induced modulation of the energy barrier at the oxide/AE interface, acting as a Schottky-like diode, which regulates the electron transport in the VCM cell. The current i_m, flowing through the ReRAM device, is then equivalent to the Schottky diode current i_{diode}. The relationship between device current i_m, voltage v_m, and memory state N_{disc} is dictated by an implicit Ohm law of the form

$$h(N_{disc}, v_m, i_m) = 0 \tag{2}$$

which bifurcates into a couple of involved expressions. One of them, due to thermal emission over a forward-biased Schottky junction, applies for the positive polarity of the device voltage, that is, over a RESET transition. Differently, the other one, due to tunneling via thermionic field emission through a reverse-biased Schottky junction, holds true for the negative polarity of the device voltage, that is, over a SET transition. Importantly, being responsible for the self-heating positive (self-cooling negative) feedback effects, which accelerate (decelerate) the device SET and RESET transition dynamics, the internal temperature T of the filament is linearly proportional to the power $P_{el} = v_m \times i_m$ dissipated in the physical stack, according to

$$T = T_0 + R_{th} \times P_{el} \tag{3}$$

where T_0 and R_{th} denote ambient temperature and device thermal resistance, respectively.

When, in the system-theoretic analysis to follow, the voltage across $R_{contact}$ shall be subtracted from the overall device voltage v_m, the resulting expression, namely $\tilde{v}_m = v_m - R_{contact} \times i_m$, where $i_m \equiv i_{diode}$, represents the voltage across the core memristor. Moreover, in all the investigations discussed in this paper, the voltage stimulus v_s is applied directly across the VCM cell, implying $v_m \equiv v_s$. The VCM cell memristance R may be estimated as the sum of four contributions, specifically the contact $R_{contact}$, plug R_{plug}, disc R_{disc}, and Schottky junction $R_{diode} = v_{diode}/i_{diode}$ resistances. Applying a given voltage v_s across the ReRAM device, the resulting modulation in the physical stack resistance may be easily computed via $R = v_s/i_m$. Despite the implicit form of both state equation and the Ohm law, the VCM cell under study is typically controlled in voltage. In order to reflect this aspect in the model investigations, the differential algebraic equation (DAE) set in Equations (1) and (2) is numerically solved through an implicit Euler numerical integration method so as to determine the device state N_{disc} and current i_m in correspondence to the control voltage v_m for all simulation time points at once. Finally, it is instructive to note that, very recently, an analytical method was developed to reformulate the JART VCM v1 model so as to let it admit an explicit formula for the current through the ReRAM cell as a function of its memory state, namely the disc oxygen vacancy concentration, as well as of the voltage dropping across its terminals.[41]

3.2. System-Theoretic Analysis of the JART VCM v1 Model Predictions

Figure 3a shows the current– voltage characteristic of the ReRAM cell, as predicted by the JART VCM v1 model, under the hypothesis that an AC periodic triangular voltage stimulus, cycling at a sweep rate (SR) of 5 $V\,s^{-1}$, is let drop across the physical stack. With the VCM cell preliminary initialized in a HRS, over the negative input half cycle, the modulus[42] of the current is found to undergo an abrupt upsurge, as soon as the voltage, falling between the device terminals, attains a value of about −0.822 V. The indefinite increase is prevented by the limiting action of the contact resistance. Similarly, over the succeeding positive input half cycle, as soon as the voltage across the physical stack increases up to a value of about +0.818 V, the device current is found to experience a sharp decrease, before undergoing a gradual descent, as induced by the contact resistance, thereafter. Acquiring a deeper understanding of the initial positive and later negative feedback mechanisms, accompanying both the SET and RESET switching transitions of the ReRAM device, under the application of voltage stimuli across its physical stack, is not a simple task. On the other hand, a deeper insight into the complex resistance switching phenomena, emerging in the VCM cell, may be gained through the analysis of its response to DC inputs.

Figure 3b shows the model prediction of the time waveform of the modulus of the device current in response to a negative SET voltage pulse of height −1 V and rise time 1 ns, for each of three distinct relatively-low initial conditions assigned to the disc oxygen vacancy concentration N_{disc}, as provided in the caption. The qualitative behavior of the device current is similar in each of the three scenarios. After an early jump to a level, dependent upon the initial device resistance (the larger is $N_{disc,\,0}$, the more conductive is the device, and, correspondingly, the higher is such a step), occurring over the pulse rise time, the modulus of the current through the physical stack exhibits a rather slow ascent, at an initial condition-dependent rate, subsequently. However, at some point in time, known as *SET time* t_{SET}, and differing on the basis of the initial value assigned to the disc oxygen vacancy concentration, the modulus of the current through the ReRAM device undergoes a rather fast transition. Later on, at some other point in time, known as *SET saturation time* $t_{SET,\,sat}$, $|i_m|$ is found to saturate toward the very same asymptotic level, when the disc oxygen concentration attains the highest possible value in the admissible domain, for all the three scenarios, which reveals the fading memory of the VCM cell under the DC stress SET test, and agrees with the experimental observations illustrated in Figure 1c. It is important to observe, here, that in a past work[43] from the literature, the very same time instants, defining beginning and end of the abrupt SET switching regime, were respectively named $t_{delay,\,SET}$ and $t_{SET} \triangleq t_{delay,\,SET} + t_{trans,\,SET}$, with $t_{trans,\,SET}$ indicating the fast SET transition time interval. The impact of the initial condition on the rate of the slow ascent in $|i_m|$, and on the delay time stems from the highly-nonlinear switching kinetics of the device as ions migrate toward the AE during the SET transition, as revealed in previous publications.[44–47] Focusing on the slow ascent of the device current modulus after the initial jump, this originates from a correspondingly low increase rate in the disc oxygen vacancy concentration, which typically characterizes the early phase of the SET transition of a device initiated in a relatively high resistance state. However, as the oxygen vacancies slowly move toward the AE, the resistance of the physical stack undergoes a minor yet progressive reduction, which inevitably

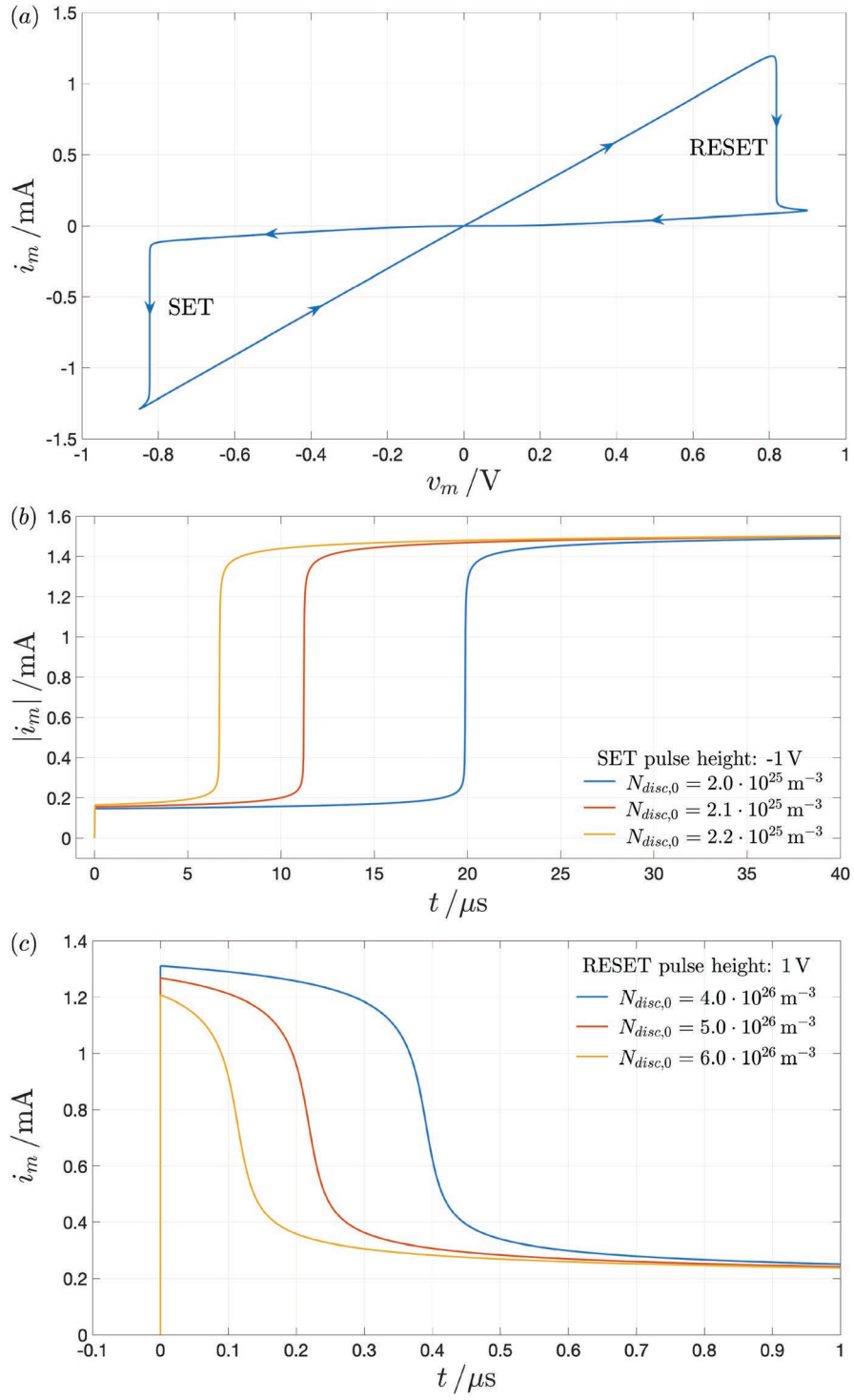


Figure 3. Predictions from the JART VCM v1 model. a) Device current i_m– voltage v_m characteristic observed under the application across the VCM cell of an AC periodic triangular voltage stimulus v_s, featuring an asymmetric shape, with minimum $v_{s,\,min}$ and maximum $v_{s,\,max}$ values equal to –0.85, and 0.9 V, respectively, and varying slowly, at a SR of 5 Vs^{-1}, that is, equivalently, at a frequency f of SR/(2 × (|$v_{s,\,min}$| + $v_{s,\,max}$)) = 1.4286 Hz). The arrows superimposed on the pinched hysteresis loop indicate the sweep direction over time. b) Time evolution of the device current modulus $|i_m|$ under a DC stress SET test, in which a negative voltage pulse, featuring a height of –1V, is let fall across the ReRAM device, for all times following its 1 ns-long rise time, for three different values assigned to the initial disc oxygen vacancy concentration $N_{disc,\,0} \triangleq N_{disc}(0)$, specifically 2×10^{25}, 2.1×10^{25}, and 2.2×10^{25} m^{-3}. c) Time evolution of the device current i_m under a DC stress RESET test, in which a positive voltage pulse, featuring a height of 1 V, is let drop between the VCM cell terminals, for all times, which follow its 1 ps-long rise time, for three distinct initial conditions assigned to the disc oxygen vacancy concentration N_{disc}, namely 3×10^{26}, 4×10^{26}, and 5×10^{26} m^{-3}.

raises the current flowing through it. The resulting increases in the temperature inside the filament increments the ion drift velocity. This speeds up the device switching transition, which further reduces the resistance of the VCM cell, activating a positive feedback mechanism, which finally leads to a dramatic upsurge in the current through its various layers.[38–41,43–48] If no measure were set in place to limit the device current, this process would finally cause an irreversible damage to the physical stack. In regard to the ReRAM device, fabricated in house at the PGI-7 facilities of the Forschungszentrum Jülich (FZJ), it is the internal series resistance R_{contact}, which prevents an uncontrollable runaway of the current in the stress SET test, as discussed in previous publications.[36] As the device current attains high levels, the consequent progressive increase (decrease) in the voltage drop across the contact resistance (across the core memristor), due to the voltage division rule, activates a negative feedback mechanism, whereby the power dissipated in the cell, due to Joule heating, reduces over time, which inevitably slows down the SET switching transition. It is clear that the filament temperature T plays a key role in both the positive and negative feedback mechanisms affecting the device dynamics during the SET transition (the interested reader is invited to consult Section S4, Supporting Information, for further insights).

Figure 3c depicts the time evolution of the device current, as observed in a numerical simulation of the Jülich Aachen Resistive Switching Tools (JART) VCM v1 model, under the specification of a RESET voltage stimulus in the form of a positive pulse of height 1 V and rise time 1 ps, for each of three different relatively-high initial values assigned to the disc oxygen vacancy concentration N_{disc} (see the caption for details).

The time course of the device current is similar for each of the three scenarios. Initially, during the pulse rise time, the current flowing through the VCM cell experiences a fast increase to an initial condition-dependent level (the larger is $N_{\text{disc, 0}}$, and the higher is the increment in i_{m}). Afterward, the current through the physical stack undergoes a slow descent at a rate dependent upon the initial condition. It is then found to exhibit an abrupt decrease at some point in time, which we call *RESET time* t_{RESET}, and is found to depend upon the initial resistance programmed into the device. However, later on, at some other point in time, known as RESET saturation time $t_{\text{RESET, sat}}$, the RESET transition rate is subject to a significant reduction, which explains the rather gradual concurrent decrease in the device current i_{m}. Importantly, this results in the asymptotic appearance of a unique steady state for the cell current, which, irrespective of the initial condition, eventually approaches a constant level, when the disc oxygen vacancy concentration N_{disc} attains the highest possible value in the admissible domain. This confirms the emergence of fading memory effects in the device under the DC stress RESET test, confirming the experimental observation illustrated in Figure 1d. Similarly as pinpointed for the SET transition scenario, earlier on, it is relevant to note, here, that in a previous publication,[43] the very same time instants, which mark beginning and end of the abrupt RESET switching regime, were respectively named $t_{\text{delay, RESET}}$ and $t_{\text{RESET}} \triangleq t_{\text{delay, RESET}} + t_{\text{trans, RESET}}$, with $t_{\text{trans, RESET}}$ indicating the fast RESET transition time interval.

Focusing now on the slow initial condition-dependent rate of decrease in the device current, which follows its initial abrupt upsurge, it can be explained through the voltage division between the contact resistor and the core memristor.[36,43,49] In fact, at the beginning of this phase, a large fraction of the voltage, corresponding to the pulse height, falls across the internal series resistance. As a result, the remainder of the stimulus voltage provides a weak force to drive the ReRAM device resistance increase. However, as the VCM cell slowly resets, the portion of the input voltage falling across the core memristor progressively increases. This results in an inevitable increase in the RESET transition speed over time. Joule heating effects accelerate the device switching dynamics further, and a positive feedback mechanism sets in, explaining the sharp decrease in the current through the physical stack. However, at some point in time, most of the input voltage is found to fall across the core memristor. Negligible further increments in the voltage across the physical stack are thus appreciated, thereafter. Since a reduction in the device current is still noticeable, the resulting decrease in the power, dissipated in the physical stack, progressively cools down the filament, reducing its temperature. In its turn, this decelerates the device RESET switching process over time.[50,51] Such a negative feedback mechanism explains the gradual phase of the RESET transition over the last part of the DC stress RESET test. It is clear that the filament temperature T plays a key role also in both the positive and negative feedback mechanisms affecting the device dynamics during the RESET transition (the interested reader is invited to consult Section S4, Supporting Information, for further insights). It is instructive to note that, in practice, ion diffusion mechanisms, due to oxygen vacancy concentration gradients across the physical stack, also play a role in the time behavior of the device current, especially under the DC stress RESET test, where they counteract the ion drift process effects. In fact, the final value attained by the current, flowing through the physical stack, under a DC stress RESET test, depends upon the balance between the ion drift toward the OE, as modulated by the electric field, and the counteractive ion diffusion toward the AE, due to the accumulation of oxygen vacancies in the most conductive region of the VCM cell.[51–53] Since the JART VCM v1 model does not account for ion diffusion mechanisms, its later development, known as JART VCM v2,[54] will be employed in a later publication to explore how the fading memory of the ReRAM device may be best leveraged for future electronics applications.

Comparing the model numerical simulations, discussed in this section, with the experimental data analyzed in Section 2, it is clear that the JART VCM v1 model is capable to reproduce rather well the dynamics of the ReRAM cell in both the DC and AC modes. This provides clear evidence for the reliability of the device model analysis to follow here and in the remainder of the manuscript. In order to allow for a thoroughly comprehensive analysis of the device nonlinear dynamics, its SET and RESET switching transitions under negative and positive pulse voltage stimuli, respectively, are studied in Sections 3.2.1 and 3.2.2, respectively, on the basis of system-theoretic investigations of the JART VCM v1 model and of its numerical integrations, over the entire variation range for the disc oxygen vacancy concentration N_{disc}, namely from $N_{\text{disc, off}} = 1 \times 10^{24}$ m^{-3} to $N_{\text{disc, on}} = 3 \times 10^{27}$ m^{-3}.

3.2.1. System-Theoretic Analysis of the SET Process

Figure 4a illustrates the time course of the device current modulus $|i_m|$ under the application of the same negative SET voltage pulse of height –1 V, as defined for the simulations from Figure 3b, for a very wide set of initial conditions, preliminarily assigned to the disc oxygen vacancy concentration. The association between each of the 15 distinct traces in Figure 4a and the corresponding initial condition may be inferred from the color coding map illustrated as legend. Importantly, here a logarithmic scale is chosen to report values on the time axis, which enables to visualize the dynamical behavior of the current for all initial conditions. Inspecting the various curves in Figure 4a, all of them exhibit an initial fast increase to an initial condition-dependent level (the higher is $N_{disc,\,0}$, the larger is the increment in $|i_m|$), as it was observed in the simulations of Figure 3b, as well as in the experiments of Figure 1c, during the pulse rise time. Subsequently, all traces feature a slow increase at some initial condition-dependent pace (the ascent in $|i_m|$ is slower and slower as the resistance, initially programmed into the VCM cell, is higher and higher). After this phase, except for the two highest initial conditions from the legend, the VCM cell is found to enter an *abrupt SET switching regime*. At each time t, within such a regime, the device current upsurge is so significant to satisfy the constraint

$$\left|\mathrm{d}i_m/\mathrm{d}\log_{10}(t)\right| \geq 10^{-4}\,\mathrm{A s^{-1}} \tag{4}$$

with

$$N_{disc,off} < N_{disc} < N_{disc,on} \tag{5}$$

that is, while, concurrently, N_{disc} lies within the bounds of its admissible existence domain $\mathcal{D}$. In the definition of an appropriate abrupt SET switching regime measure, the device current in Equation (4) is differentiated with respect to the base-10 logarithm of the time, which allows to express through an ad hoc mathematical formula the slope visualizable along each of the traces, plotted on a logarithmic time scale, in Figure 4a. An asterisk marker indicates the first point in time, earlier referred to as SET time t_{SET}, at which the inequality in Equation (4) holds true, for each of the traces, except those associated to the two largest initial conditions from the legend. For these two initial conditions, in fact, it is not possible to identify, clearly, a point in time, at which the modulus of the derivative of the device current with respect to the time, expressed in logarithmic scale, attains the threshold of 10^{-4} A s^{-1}, as established by the inequality in Equation (4). Under these circumstances, the entire on-switching process appears rather gradual, which allows to tune the VCM cell resistance finely in a potential experiment. Importantly, for all initial conditions, where the ReRAM device is found to enter an abrupt switching regime, the lower is $N_{disc,\,0}$, and the larger is the set time t_{SET}. Importantly, t_{SET} is found to span over 17 orders of magnitude in time, which provides clear evidence for the strongly-nonlinear on-switching kinetics of the VCM cell. Furthermore, for each trace, which hosts an asterisk marker, except for the curves corresponding to the three lowest initial conditions from the legend in Figure 4a, the abrupt switching phase is followed by another gradual one. In fact, analyzing the time series of the device current modulus in each of these SET transition scenarios, a further initial condition-dependent point in time, earlier referred to as SET saturation time $t_{SET,\,sat}$, may be identified (refer to the square marker), at which the inequality in Equation (4) holds true with $N_{disc} < N_{disc,\,on}$, that is, under the hypothesis expressed by Equation (5). At the SET saturation time the physical stack is found to enter a new gradual switching phase, referred to as *SET saturation regime*, where further increments in $|i_m|$ are limited by the presence of the internal series resistance $R_{contact}$. The SET saturation regime may not be identified on either of the three rightmost traces, since, in each of these cases, the disc oxygen vacancy concentration attains the upper bound in its existence domain, while the inequality in Equation (4) still holds true.

As a further aspect of interest, the increment in the device current modulus over the abrupt phase, as may be estimated for all traces, which host both an asterisk and a square marker, differs from initial condition to initial condition. In fact, inspecting Figure 4a, it is clear that the vertical distance between the asterisk and square markers varies across these traces. It increases as the resistance initially programmed into the device increases, which means that $t_{SET,sat} - t_{SET}$ actually gets larger and larger as the value assigned to $N_{disc,\,0}$ is smaller and smaller. As an additional significant note, with reference to Figure 4a, it is worth to observe that, from each of the initial conditions, the device current modulus eventually attains a constant level, which is determined uniquely by the device voltage and by the unique asymptotic value of the disc oxygen vacancy concentration, namely $N_{disc,\,on}$, as established by the implicit Ohm law (Equation (2)). Section S4, Supporting Information, file visualizes the time evolution of other physical variables of interest, specifically the filament temperature T, and the voltages $\tilde{v}_m$, and $v_{contact}$, falling across core device and contact series resistance, respectively, as recorded during each of the numerical simulations, which resulted in the $|i_m|$ versus t loci of Figure 4a.

In order to gain a deeper understanding of the resistance switching phenomena, emerging in the physical stack under the DC stress SET test, it is important to analyze the device dynamics along its state dynamic route (SDR) for a negative DC voltage V_m, let fall between its two terminals, of value equal to the pulse height, here set to –1 V. Given that a negative DC voltage stimulus induces a SET transition in the ReRAM cell, a SDR, associated to a negative-valued V_m, is also referred to as *SET SDR*. Grouping a number of SET SDRs, one for each negative DC voltage, let fall across the ReRAM cell, the resulting family of loci forms the device SET DRM. As discussed later on in Section 3.2.2, a complementary family of loci, referred to as RESET DRM, allows to gain insights into the device resistance switching transitions under positive DC voltage stimuli (see Section S3, Supporting Information, file for more details about the system-theoretic graphic tool called DRM, which obviously combines together both the SET and the RESET DRMs). As established by the ReRAM cell state Equation (1), the locus of $|\mathrm{d}N_{disc}/\mathrm{d}t| \equiv \mathrm{d}N_{disc}/\mathrm{d}t$ versus N_{disc} for $V_m = -1$ V is illustrated in Figure 4b. Since the disc oxygen vacancy concentration N_{disc} is unaccessible in practice, it is insightful to introduce a current-based variant of each SET SDR, which we call SET current dynamic route (CDR), and define as the locus of the modulus of the time derivative of the device current $|\mathrm{d}i_m/\mathrm{d}t| \equiv \mathrm{d}|i_m|/\mathrm{d}t$

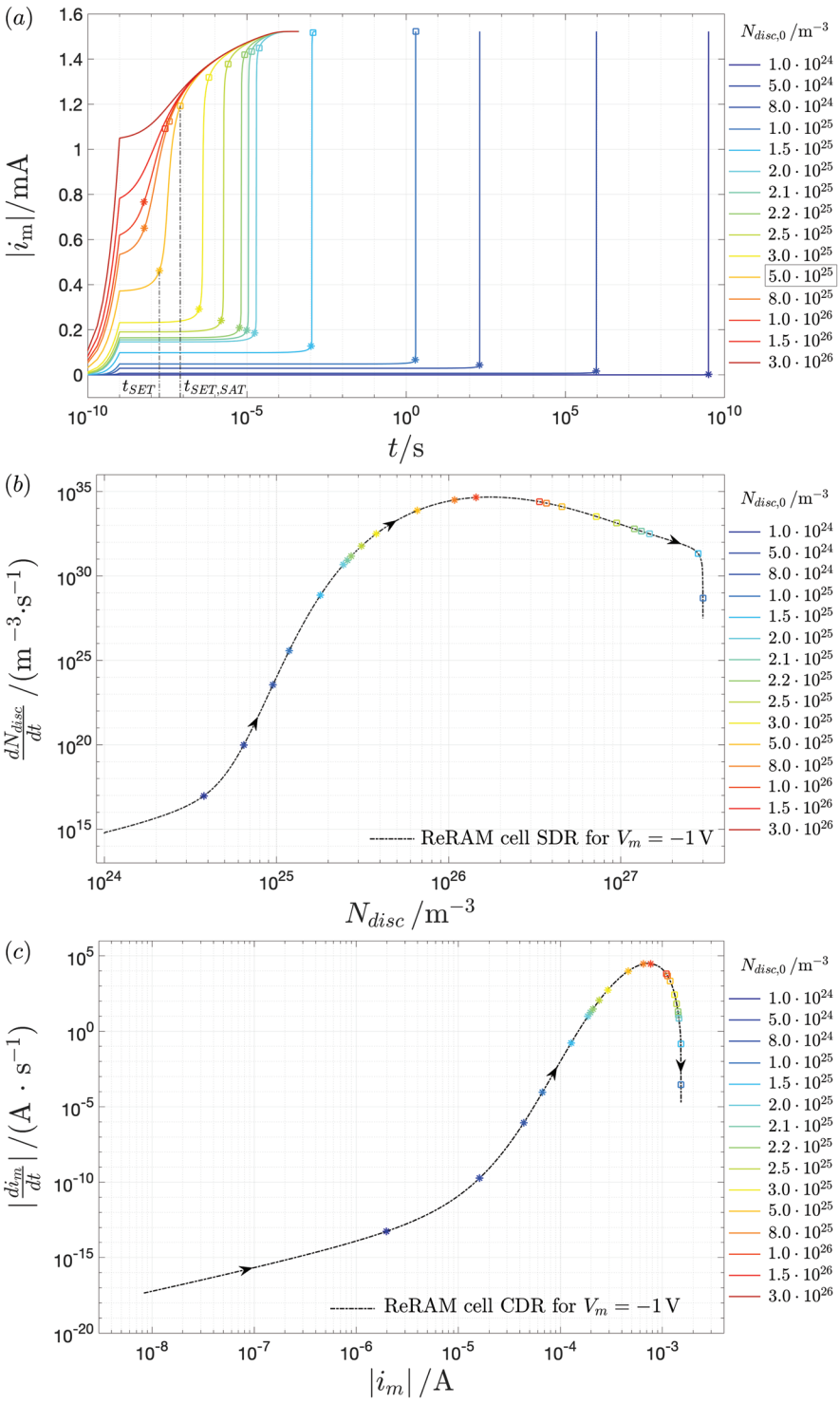


Figure 4. System-theoretic analysis of the JART VCM v1 model predictions of the device response to negative DC voltage excitations. a–c) Investigation of a DC stress SET test, in which a voltage source, generating a negative pulse of height –1 V and rise time 1 ns, is inserted in parallel to the VCM cell for 15 different values assigned to its initial disc oxygen vacancy concentration $N_{disc,\,0}$, as reported in the common legend from either of the plots. a) Time evolution of the device current modulus $|i_m|$. b) dN_{disc}/dt versus N_{disc} locus of the VCM cell for $V_m = -1$ V. In system-theory, an arrowed locus of this kind is known as a SDR. Since here the DC voltage across the ReRAM cell induces its SET transition, a SDR of this kind is referred to as a *SET SDR*. c) $|di_m/dt|$ versus $|i_m|$ locus of the VCM cell, for $V_m = -1$ V. An arrowed locus of this kind is a current-based variant of a SET SDR, referred to as *SET current dynamic route (SET CDR)*. In each plot from the triplet (a– c), an asterisk and a square, sharing the same color, mark beginning and end of the abrupt switching phase in the device SET transition. Referring to plot (a), for the current trace associated to the initial condition, shown within a rectangular frame on the respective legend, specifically $N_{disc,\,0} = 5 \times 10^{25}$ m^{-3}, the SET time t_{SET} and the SET saturation time $t_{SET,\,sat}$ are clearly marked as abscissas of the asterisk and square markers, respectively.

versus the device current modulus $|i_m|$ for a given negative bias value assigned to the voltage V_m across the physical stack. *This novel graphic tool is intended to enable the application of the system-theoretic analysis method, centered on the DRM graphic tool, to data measured from device samples, in future research investigations, where a family of SET CDRs, one for each negative V_m value of interest, would be recorded to form a SET current dynamic route map (SET C-DRM).*

Figure 4c depicts the CDR of the VCM cell for $V_m = -1$ V, as it descends from the device DAE sets in Equations (1) and (2). As it is the case under any negative DC voltage, the sign of the time derivative of the disc oxygen vacancy concentration (device current modulus) keeps positive for all admissible N_{disc} ($|i_m|$) values over a SET transition, as indicated by the eastward direction of the arrows superimposed on the SET SDR (SET CDR) from plot (b) ((c)) in Figure 4. This implies that the device may asymptotically exhibit one and only one possible steady-state behavior, sitting on its lowest admissible resistance state, as inferable from Figure 4a, provided the stimulus were not removed beforehand. With reference to Figure 4, processing the numerical data, extracted from all the DC stress SET tests, which resulted in the traces from Figure 4a, from the end of the pulse rise time, for each of the initial conditions the trajectory point (N_{disc}, dN_{disc}/dt) ((i_m, $|di_m/dt|$)) draws over time a path, which lies entirely on the SDR (CDR) from plot (b) ((c)), and terminates eventually on its rightmost location, where the device attains the lowest possible resistance state.

It is instructive to note that there exists a specific one-to-one function, which maps the disc oxygen vacancy concentration to the device current modulus for each negative DC voltage let fall across the physical stack. Such a function, which does not have a closed-form expression, but can nevertheless be numerically derived from the implicit Ohm law (Equation (2)), is highly nonlinear. This notwithstanding, the SET SDR and SET CDR, shown in Figure 4b,c, respectively, share common features. First of all, as anticipated earlier, the sign of the time derivative of the disc oxygen vacancy concentration (device current modulus) is positive throughout the admissible variation range for the disc oxygen vacancy concentration (device current modulus), as is the case under any other negative DC value assigned to the voltage across the physical stack. Importantly, moving from the lowest possible to the highest possible disc oxygen vacancy concentration (device current modulus), the SET SDR (CDR) of the VCM cell for $V_m = -1$ V, as shown in Figure 4a(b), undergoes a monotonic increase up to a maximum, and decreases monotonically, thereafter. Moreover, the region to the left of the hump in the SET SDR (SET CDR) from plot (b) ((c)), where the positive-valued time derivative of the disc oxygen vacancy concentration (device current modulus) gets larger as N_{disc} ($|i_m|$) increases, defines the domain, where positive feedback mechanisms, due to Joule heating effects, accelerate the device dynamics during the SET transition under $V_m = -1$ V. On the other hand, the region to the right of the hump in the SET SDR (SET CDR) from plot (b) ((c)), where the positive-valued time derivative of the disc oxygen vacancy concentration (device current modulus) gets smaller as N_{disc} ($|i_m|$) increases, defines the domain, where negative feedback mechanisms, due to the limiting action exerted by the series resistor, decelerate the device dynamics during the SET transition under $V_m = -1$ V. Now, as a further aspect of interest, if the trajectory point (N_{disc}, dN_{disc}/dt) (($|i_m|$, $|di_m/dt|$)), which is sampled directly at the end of the pulse rise time, when the voltage across the VCM cell is first found to be equal to –1 V, lies to the right of the hump, only negative feedback mechanisms affect the device SET transition, which may appear gradual throughout the DC stress SET test. Conversely, if this very same trajectory point lies to the left of the hump, then, at some stage, the device dynamics are accelerated by thermal effects, which explains why, in a scenario of this kind, the device is found to enter an abrupt switching regime, as defined in Equation (4). While, at first glance, with reference to the SET SDR from Figure 4b (the SET CDR from Figure 4c), one could conclude that, when N_{disc} ($|i_m|$) visits points at positive/negative slope, the device undergoes abrupt/gradual switching transition, this is not always the case, according to the measure established via inequality in Equation (4). In order to clarify this point, for each of the initial conditions, from which the device enters an abrupt regime, as established by such inequality, the SET time t_{SET}, and, if it exists, the SET saturation time $t_{SET,\,sat}$, are respectively marked along the associated SET SDR from Figure 4b as well as along the associated SET CDR from Figure 4c, similarly as indicated in Figure 4a, that is, through an asterisk and a square marker of relevant initial condition-dependent color (the color coding map, graphically illustrated as legend in Figure 4a, is reported for reference also adjacent to each of Figure 4b,c).

Very importantly, according to the nonlinear mapping, which relates N_{disc} and $|i_m|$ under $V_m = -1$ V, the current modulus, which corresponds to the disc oxygen vacancy concentration, at which the SET SDR from Figure 4b features a maximum, is approximately the same value as the abscissa of the maximum in the SET CDR from Figure 4c. With this in mind, let us now focus on any of the 13 initial conditions, from which the device is found to enter an abrupt regime, according to the measure from inequality in Equation (4), and follow the evolution of the respective disc oxygen vacancy concentration (current modulus) on the SET SDR (SET CDR) of Figure 4b(c). In each of these cases, the trajectory point (N_{disc}, dN_{disc}/dt) (($|i_m|$, $|di_m/dt|$)) first enters the path established by the SET SDR (SET CDR) from plot (b) ((c)) to the left of its hump. From that time instance, and while the trajectory point (N_{disc}, dN_{disc}/dt) (($|i_m|$, $|di_m/dt|$)) keeps to the left of the hump of the respective SET SDR (SET CDR), N_{disc} ($|i_m|$) first experiences a slow increase, and then an abrupt upsurge. Importantly, the device keeps in the abrupt regime also during part or all of the descent of the trajectory point (N_{disc}, dN_{disc}/dt) (($|i_m|$, $|di_m/dt|$)) along the route at negative slope to the right of the hump of the SET SDR (SET CDR) of Figure 4b(c), for ten and three of the 13 scenarios under consideration, respectively. This observation shows that the existence of a hump on the SET SDR (SET CDR), associated to a given negative DC voltage, constitutes a necessary condition for the device to undergo three main phases in the underlying SET process, namely two gradual transitions, separated by an abrupt one, provided the resistance state of the ReRAM device at the time, when the physical stack is first subject to the fixed negative voltage stimulus, corresponds to a disc oxygen vacancy concentration (device current modulus), which lies to the left of

the maximum of the respective arrowed dN_{disc}/dt versus N_{disc} ($|di_m/dt|$ vs $|i_m|$) locus. However, for any scenario, where the disc oxygen vacancy concentration (device current modulus) is found to undergo an abrupt upsurge, the eventual evolution of the respective trajectory point (N_{disc}, dN_{disc}/dt) (($|i_m|$, $|di_m/dt|$)) along the path at negative slope to the right of the hump on the SET SDR (SET CDR) does not constitute a sufficient condition for the appearance of a saturation in the response of the ReRAM device in the final phase of the DC stress SET test.

The deep system-theoretic analysis, presented in this section, enables to explain certain typical observations, related to the SET process in ReRAM cells, reported in the past by device physics researchers.[43] In particular, the SET transition in memory devices of this kind may appear gradually, even during the time interval, when the modulus of the current undergoes an abrupt upsurge, if the abrupt switching regime time span becomes comparable to the SET time, that is, equivalently, adopting the terminology introduced in ref. [43], the delay time. This happens when the VCM cell features a relatively-low resistance state, when a certain constant voltage of negative polarity is first applied across its two terminals. The following remark gains a deeper insight into this important aspect.

Remark 1: Despite inequalities in Equations (4)–(5) set a rigorous absolute measure for identifying an abrupt phase in the device resistance switching transition due to the application of a given negative DC pulse voltage across the ReRAM cell, whether, in a practical lab measurement, the change in the device resistance from a higher value to a lower one would appear sharp or gradual, to the eyes of an external observer, actually depends, crucially, on the ratio between the given on-transition time interval and the time elapsed since the beginning of the experiment. Let us gain a deeper understanding. From the implicit Ohm law in Equation (2), fixing the device voltage v_m to a given negative value, as done here, each current modulus level $|i_m|$ is uniquely associated to one and only one value for the disc oxygen vacancy concentration N_{disc}, and, as a result, to one and only one value for the time derivative of the disc oxygen vacancy concentration dN_{disc}/dt. With this in mind, as, under the given negative DC voltage input, the device current modulus increases from any positive value, say $I_{m,1}$, to any other one, say $I_{m,2}$, the device switching speed is unequivocally determined by the state Equation (1), for each choice of the initial condition, which drives the device current through the target transition range $[I_{m,1}, I_{m,2}]$. As a result, the time interval, which elapses as $|i_m|$ is subject to the desired increment, is the same for each of these initial conditions. As an example, with reference to Figure 4a, each of the 15 traces increases from $I_{m,1} = 0.6$ mA to $I_{m,2} = 0.8$ mA within a common time interval. However, to the eyes of an experimenter, this very same time interval appears shorter and shorter, the higher and higher is the resistance initially programmed into the ReRAM cell. This is because, as we move from the leftmost trace to the rightmost trace in Figure 4a, the *device response time span*, defined as the time interval, over which the device current modulus is subject to the given incremental transition, becomes smaller and smaller in comparison to the *experiment time span*, defined as the delay time of the onset of the transition under consideration as compared to the time of application of the SET pulse.

3.2.2. System-Theoretic Analysis of the RESET Process

A similar analysis, as carried out for a SET transition of the VCM cell in Section 3.2.1, is now performed under a DC stress RESET test. With reference to **Figure 5**a which illustrates the time evolution of the current i_m as a positive voltage pulse of height 1 V, as specified for the simulations of Figure 3c is let to fall across the device terminals, for each of 14 different initial conditions, as indicated in the legend. A RESET SDR (RESET CDR) of the VCM cell, defined as the $|dN_{disc}/dt|$ versus N_{disc} ($|di_m/dt|$ vs $|i_m| \equiv i_m$) locus, and derived from the JART VCM v1 model, is shown in plot (b) ((c)) of the same figure for $V_m = 1$ V. Note that, as it is the case under any positive DC voltage, let fall across the physical stack, the time derivative of the disc oxygen vacancy concentration (device current) keeps negative for all possible N_{disc} (i_m) values throughout a RESET transition, as indicated by the arrows, pointing westward, drawn along the RESET SDR (RESET CDR) from Figure 5b(c). The strictly-negative polarity, which dN_{disc}/dt features under any positive DC stimulus, implies that, provided the stimulus were not removed over the course of the RESET transition, the VCM cell may asymptotically feature one and only one admissible steady-state behavior, sitting on its highest possible resistance state, which would happen way after the final time of 1 s in the simulations from Figure 5a. With reference to this plot, all the device current traces feature an initial fast increase to an initial condition-dependent level (the higher is $N_{disc,0}$, and the larger is the increment in i_m), as it was observed in the simulations of Figure 3c, as well as in the experiments of Figure 1d, during the pulse rise time. Subsequently, all traces feature a slow decrease at some initial condition-dependent pace (the descent in i_m is slower and slower as the resistance, initially programmed into the VCM cell, is lower and lower). After this phase, except for the three lowest initial conditions from the legend, the device enters an *abrupt RESET switching regime*, where, at each time instant t, its current decreases so significantly to satisfy the constraint

$$\left|di_m/d\log_{10}(t)\right| \geq 10^{-3}\ \mathrm{As}^{-1} \tag{6}$$

In the proposed abrupt RESET switching regime measure the differentiation of the device current is made with respect to the base-10 logarithm of the time. This measure allows to monitor the slope of the device current versus time locus, when the horizontal axis is scaled logarithmically, as is the case for the traces in Figure 5a.

With reference to this plot, an asterisk marker indicates the first point in time, earlier referred to as RESET time t_{RESET}, at which the inequality in Equation (6) holds true, for each of the 14 traces, except those associated to the three smallest initial conditions from the legend, where this condition is never met. Importantly, for all initial conditions, where the ReRAM device is found to enter an abrupt switching regime the higher is $N_{disc,0}$, and the larger is the RESET time t_{RESET}. Importantly, t_{RESET} is found to span over four orders of magnitude in time, which, as compared to the multi-decade variation in the SET time, demonstrates the lower degree of nonlinearity of the RESET switching kinetics of the VCM cell relative to its SET switching kinetics. Preliminarily programming the device in

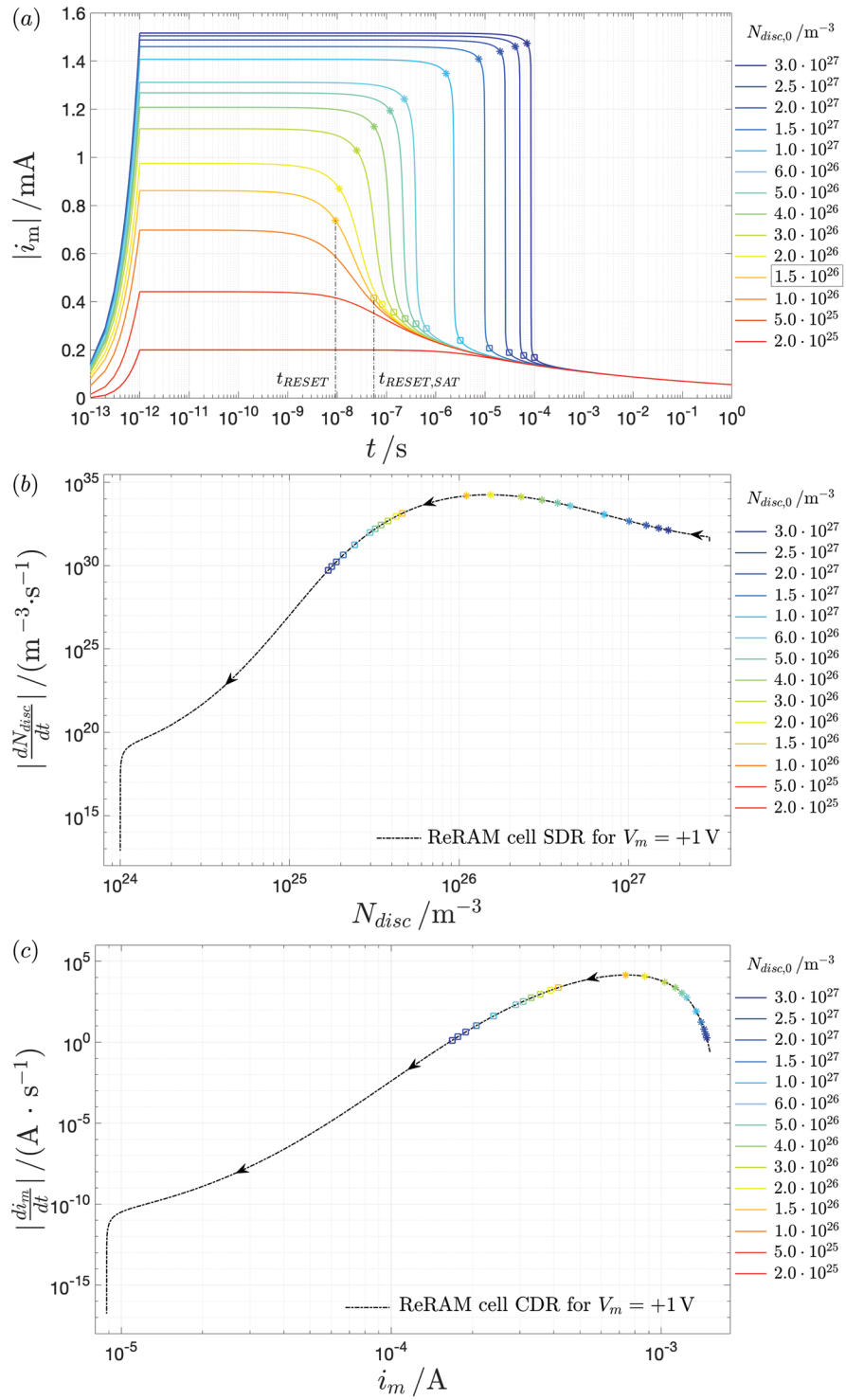


Figure 5. System-theoretic analysis of the JART VCM v1 model predictions of the device response to positive DC voltage excitations. a–c) Investigation of a DC stress RESET test, where the voltage across the VCM cell is supplied by a source, producing a pulse of height 1 V and rise time 1 ps, under 14 initial values for $N_{disc,0}$, as specified in the common legend from either of the plots. a) Time evolution of the device current i_m. b) $|dN_{disc}/dt|$ versus N_{disc} locus of the VCM cell for $V_m = 1$ V. In system-theory, an arrowed locus of this kind is known as a SDR. Since here the DC voltage across the ReRAM cell induces its RESET transition, a SDR of this kind is referred to as a *RESET SDR*. c) $|di_m/dt|$ versus i_m locus of the VCM cell for $V_m = 1$ V. An arrowed locus of this kind is a current-based variant of a RESET SDR, and is referred to as *RESET current dynamic route (RESET CDR)*. In each of the three plots (a– c), an asterisk and a square, marked in a common color, respectively indicate the onset and the conclusion of the abrupt switching phase in the device RESET transition, as computed from the numerical simulation corresponding to the associated initial condition. With reference to plot (a), for the device current trace associated to the initial condition, shown within a rectangular frame on the respective legend, specifically $N_{disc,0} = 1.5 \times 10^{26}$ m^{-3}, the RESET time t_{RESET} and the RESET saturation time $t_{RESET,sat}$ are clearly marked as abscissas of the asterisk and square markers, respectively.

either of the three highest resistance states, which correspond to the lowest initial conditions in the range, indicated in the legend of Figure 5a, it is not possible to identify, clearly, a point in time, at which the modulus of the derivative of the current with respect to the time, expressed in logarithmic scale, attains the threshold of 10^{-3} As^{-1}, as established by the inequality in Equation (6). Under these circumstances, the entire RESET switching process appears rather gradually, which allows to tune the VCM cell resistance finely in a potential experiment.

Differently from what is the case during the DC stress SET tests of Figure 4a, each trace, which hosts an asterisk marker in Figure 5a, eventually leaves the abrupt switching phase, entering a new gradual one. In fact, from the analysis of the time series of the device current in each of these RESET transition scenarios, an additional initial condition-dependent point in time may be detected (as indicated with a square marker), at which the inequality in Equation (6) is last satisfied. This time instant is referred to as *RESET saturation time* $t_{\mathrm{RESET,\,sat}}$, because, thereafter, the ReRAM cell is found to enter a new gradual switching phase, referred to as *RESET saturation regime*, where further decrements in i_{m} are limited by the cooling of the filament, due to the progressive reduction in the power dissipated in the physical stack. As a further aspect of interest, the duration of the abrupt switching regime, defined as $t_{\mathrm{RESET,\,sat}} - t_{\mathrm{RESET}}$, depends crucially upon the resistance initially programmed into the device, and, particularly, increasing for larger values assigned to $N_{\mathrm{disc,\,0}}$. As an additional note, differently from what happens during a SET transition (see Figure 4a), any trace from Figure 5a converges to the same solution well before the device shows a unique steady-state behavior, when the disc oxygen vacancy concentration N_{disc} attains the lower bound $N_{\mathrm{disc,\,off}}$ in its existence domain, and the ReRAM cell features the highest possible resistance. Section S4, Supporting Information, visualizes the time evolution of other physical variables of interest, specifically the filament temperature T, and the voltages $\tilde{v}_{\mathrm{m}}$, and v_{contact}, falling across core device and contact series resistance, respectively, as recorded during each of the numerical simulations, which resulted in the $|i_{\mathrm{m}}|$ versus t loci of Figure 5a.

Processing the numerical data in Figure 5a allows us to gain a deeper insight into the RESET switching transition of the device physical stack, preliminary initialized into any of the resistance states, inferable from the legend, in response to the aforementioned 1 V-high positive voltage pulse stimulus. The aim is to analyze the time evolution of the trajectory point $(N_{\mathrm{disc}},\ |\mathrm{d}N_{\mathrm{disc}}/\mathrm{d}t|)$ $((i_{\mathrm{m}},\ |\mathrm{d}i_{\mathrm{m}}/\mathrm{d}t|))$ on the unique RESET SDR (RESET CDR) of the VCM cell, corresponding to a fixed unitary value assigned to the device voltage, from the first point in time, at which the source voltage v_{s} attains its final value, that is, directly after the pulse rise time.

As was the case for any SET transition, for each positive DC voltage across the ReRAM device, there exists a specific one-to-one map between the disc oxygen vacancy concentration and the current through the physical stack. Despite the nonlinearity of the map, the RESET SDRs of Figure 5b and RESET CDRs of Figure 5c share common characteristics. First, the sign of $\mathrm{d}N_{\mathrm{disc}}/\mathrm{d}t$ $(\mathrm{d}i_{\mathrm{m}}/\mathrm{d}t)$ is negative for all values, which N_{disc} (i_{m}) may ever assume during the RESET transition. Importantly, moving from the highest possible to the lowest possible disc oxygen vacancy concentration (device current), the RESET SDR (RESET CDR) of the VCM cell for $V_{\mathrm{m}} = 1$ V, as shown in Figure 5b(c), undergoes a monotonic increase up to a maximum, and decreases monotonically thereafter. Moreover, the region to the right of the hump in the RESET SDR (RESET CDR) from plot (b) ((c)), defines the domain, where positive feedback mechanisms, due to the series resistor-core memristor voltage division, inducing self-heating effects in the ReRAM cell, as the resistance of its physical stack progressively increases, accelerate the device dynamics during the RESET transition under $V_{\mathrm{m}} = 1$ V. On the other hand, the region to the left of the hump in the RESET SDR (RESET CDR) from plot (b) ((c)) defines the domain, where negative feedback mechanisms, due to the progressive decrease, which the power, entering the ReRAM cell undergoes, when the current through the physical stack drops more than the ongoing increase in the voltage between its terminals, decelerate the device dynamics during the RESET transition under $V_{\mathrm{m}} = 1$ V.

Now, if the trajectory point $(N_{\mathrm{disc}},\ |\mathrm{d}N_{\mathrm{disc}}/\mathrm{d}t|)$ $((i_{\mathrm{m}},\ |\mathrm{d}i_{\mathrm{m}}/\mathrm{d}t|))$, which is sampled directly at the end of the pulse rise time lies to the left of the hump, only negative feedback mechanisms affect the RESET transition, which may appear gradually throughout the DC stress RESET test. Conversely, if this very same trajectory point lies to the right of the hump, then, at some stage, the device dynamics are accelerated as a progressively larger portion of the stimulus bias voltage drops across the core memristor, which explains why, in a scenario of this kind, the device is found to enter an abrupt switching regime, as defined in Equation (6). While, at first glance, with reference to the RESET SDR (RESET CDR) from Figure 5b(c), one could conclude that, when N_{disc} (i_{m}) visits points at negative (positive) slope, the device undergoes an abrupt (a gradual) switching transition, this is not always the case, according to the measure established via inequality in Equation (6).

In order to clarify this point, for each of the initial conditions, from which the device enters an abrupt regime, established by the inequality in Equation (6), the RESET time t_{RESET}, and the RESET saturation time $t_{\mathrm{RESET,\,sat}}$, are marked in the RESET SDR from plot (b) (RESET CDR from plot (c), similarly as indicated in plot (a), that is, through an asterisk and a square marker of relevant initial condition-dependent color. The same color coding map, graphically illustrated as legend in plot (a), is reported for reference also alongside each of plots (b) and (c).

Very importantly, according to the nonlinear mapping, which relates N_{disc} and i_{m} under $V_{\mathrm{m}} = 1$ V, the device current, which corresponds to the disc oxygen vacancy concentration, at which the RESET SDR from plot (b) features a maximum, is approximately the same value as the abscissa of the maximum in the RESET CDR from plot (c).

With this in mind, let us now focus on any of the 11 initial conditions, from which the device is found to enter an abrupt regime, and follow the evolution of the respective disc oxygen vacancy concentration (device current) on the RESET SDR (RESET CDR) of Figure 5b(c) directly after the pulse rise time. In each of these cases, the trajectory point $(N_{\mathrm{disc}},\ |\mathrm{d}N_{\mathrm{disc}}/\mathrm{d}t|)$ $((i_{\mathrm{m}},\ |\mathrm{d}i_{\mathrm{m}}/\mathrm{d}t|))$ first enters the path established by the RESET SDR (RESET CDR) from plot (b) ((c)) to the right of its hump. From that time instant, and while the trajectory point $(N_{\mathrm{disc}},\ |\mathrm{d}N_{\mathrm{disc}}/\mathrm{d}t|)$ $((i_{\mathrm{m}},\ |\mathrm{d}i_{\mathrm{m}}/\mathrm{d}t|))$ keeps to the right of the hump of the respective RESET SDR (RESET CDR), N_{disc} (i_{m}) first experiences a slow descent, and then an abrupt decrease. Importantly, the device keeps in the abrupt regime also during part of the

descent of the trajectory point (N_{disc}, $|dN_{disc}/dt|$) ((i_m, $|di_m/dt|$)) along the route at positive slope to the left of the hump of the RESET SDR (RESET CDR) of Figure 5b(c) for each of the 11 scenarios under consideration. This observation shows that the existence of a hump on the RESET SDR (RESET CDR), associated to a given positive DC voltage, let fall across the VCM cell, constitutes a necessary condition for the device to undergo three main phases in the underlying RESET process, namely two gradual transitions, separated by an abrupt one, provided the resistance state of the ReRAM device, at the time, when the physical stack is first subject to the fixed positive voltage stimulus, corresponds to a disc oxygen vacancy concentration (device current), lying to the right of the hump. Moreover, as compared to the curvature around the respective maximum and the multi-decade modulation in dN_{disc}/dt ($|di_m/dt|$) for the SET SDR (SET CDR) for $V_m = -1$ V from Figure 4b(c), the RESET SDR (RESET CDR) for $V_m = +1$ V from Figure 5b(c) is flatter in the region around the respective hump, which reduces the range of variation for $|dN_{disc}/dt|$ ($|di_m/dt|$) across the allowable set of values, which N_{disc} (i_m) may ever assume over a RESET transition under the unitary bias voltage stimulus. This explains why, for any RESET transition scenario from Figure 5a, where the disc oxygen vacancy concentration (device current) is found to undergo an abrupt decrease, eventually a saturation in the response of the ReRAM device appears, before the device attains its highest possible resistance state. The thorough system-theoretic analysis, reported in this section, allows to explain phenomena observed in experimental RESET tests on ReRAM cells. Specifically, the RESET transition in memory devices of this kind may appear gradual, even over the time interval, when the current through the physical stack undergoes an abrupt decrease, provided the VCM cell features a relatively-high resistance state, when, first, a certain constant voltage of positive polarity is let fall across its two terminals, which ensures that the abrupt switching regime time span is comparable to the RESET time, that is, equivalently, adopting the terminology introduced in ref. [43], the delay time. In fact, the above remark on the impact of the time span of the experiment on the speed of the SET switching transition holds its validity for the RESET switching process as well. Particularly, for a given positive DC voltage V_m, let fall across the VCM cell, the time necessary for observing a decrement in its current i_m from any positive value, say $I_{m,1}$, to any other one, say $I_{m,2}$, is independent of the initial condition, which drives the device current through the desired transition range. However, whether, during a laboratory measurement, under the given positive bias voltage stimulus, the transition of the device current from the upper value to the lower one in the range $[I_{m,1}, I_{m,2}]$ would appear gradual or abrupt to the eyes of an external observer depends critically upon the ratio between the experiment time span, that is, the delay time of the onset of the transition under focus, and the *device response time span*, defined as the time interval, over which the device current is subject to the target decrement. In fact, with reference to Figure 5a, the lower is the resistance, initially programmed into the ReRAM cell, and the higher is such a time span ratio, which explains why, to the eyes of an experimenter, the device response would appear faster.

In conclusion, on the basis of the analysis carried out in Sections 3.2.1 and 3.2.2, some conclusions, on proper memristive device modeling, may be drawn. In order to reproduce the transition of the response of a ReRAM cell, preliminary programmed into a relatively-high (relatively-low) resistance state, to a SET (RESET) negative (positive) voltage pulse stimulus of given height from a runaway phase to a saturation regime, the respective system-theoretic SET (RESET) SDR, or its device current-based variant, that is, the SET (RESET) CDR, must necessarily feature a hump, which separates a positive feedback region, to its left (right), from a negative feedback one, to its right (left).

Whether the resistance switching process, which the device undergoes under a DC stress test, appears gradual or abrupt, depends crucially upon the ratio between the experiment and device response time spans. However, as explained earlier, irrespective of the initial condition, under a RESET transition, at some point in time, the device is found to enter a final gradual switching phase well before attaining its asymptotic resistance state, differently from what happens, in general, during a SET transition. This explains why it is easier to control the RESET process than the SET transition. In order to capture this asymmetry between the on and off switching dynamics, it is necessary that each given system-theoretic RESET SDR, or its device current-based variant, that is, the associated RESET CDR, feature a flatter region around the respective hump, allowing for a narrower range of variation for the switching speed, as compared to the corresponding system-theoretic SET SDR, or its device current-based variant, that is, the associated SET CDR.

Finally, since the onset and end of the abrupt switching regime, as defined by the inequalities in Equations (4) and (5) (inequality in Equation (6)) under a DC stress SET (RESET) test, may be extracted by processing the time series of the device current, which is recordable in the lab, the criterion, proposed in this manuscript to identify the abrupt transition phase, may be used for fitting a mathematical model to experimental data. As a yet-open issue, the relationship between a system-theoretic SET or RESET SDR and its current-based variant, that is, the corresponding SET or RESET CDR, is ambiguous, unless a map between the internal state of the ReRAM device and its current, for each possible negative or positive voltage, dropping across its terminals, may be unequivocally determined.

4. Memory Loss in the Periodically-Driven VCM Cell

Having comprehensively studied the fading memory effects, which accompany the resistance switching phenomena, emerging in the ReRAM device under a DC stress test, we are now ready to investigate the memory loss induced in the physical stack by purely-AC periodic voltage stimuli, where the adverb "purely" is used to indicate that the inputs, under consideration in the investigations to follow, are bound to feature a null time average. At this point, it is important to remark that, since the analysis of AC fading memory effects in the memory device constitutes the main focus of the manuscript, the JART VCM v1 model, employed in all the numerical investigations carried out in this research work, was preliminarily fitted to measurement data, extracted from a particular sample under experiments testing the capability to erase the past history of the respective physical stack by means of periodic stimulation.

4.1. Experimental and Numerical Evidence for the Fading Memory of the ReRAM Cell under Purely-AC Periodic Excitation

Both, lab measurements on a ReRAM cell and numerical simulations of the JART VCM v1 model reveal the emergence of fading memory effects in the periodically-forced memristive system.

Figures 6 and **7** show the corresponding results for the experiment and the numerical simulation, respectively. To this end, the device was initialized into three distinct resistance states (the three corresponding disc oxygen vacancy concentrations), specifically $R_0 \triangleq R(0) \in \{910, 10800, 16600\}\Omega$ ($N_{\text{disc},0} \in \{3\times10^{27}, 76\times10^{24}, 33\times10^{24}\}\text{m}^{-3}$). The application of a purely-AC periodic triangular voltage stimulus v_s of amplitude

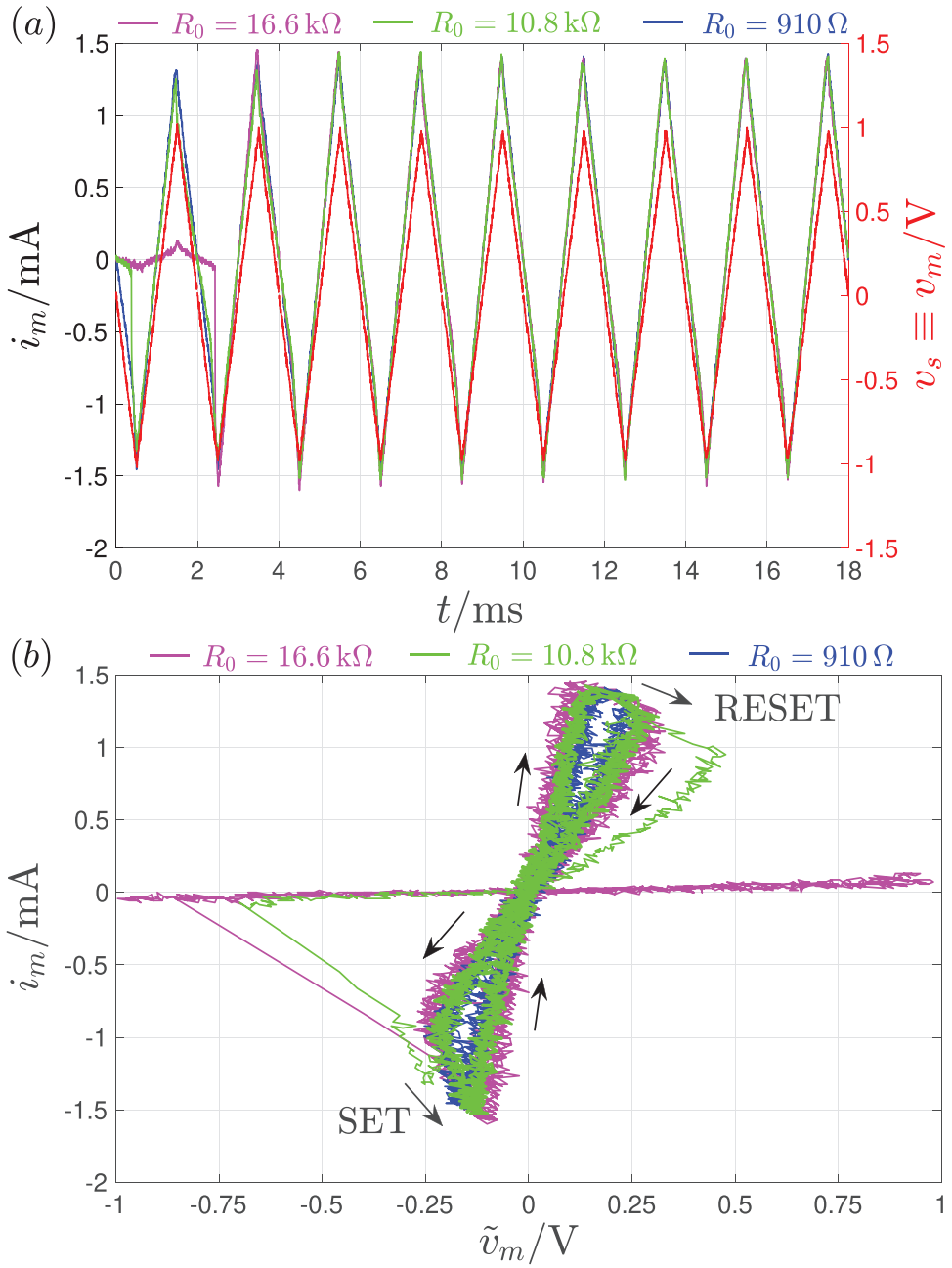


Figure 6. Experimental demonstration of fading memory effects in the resistance switching response of the periodically-driven TaO_x ReRAM device. a) Purely-AC periodic triangular voltage v_s of amplitude $\hat{v}_s = 1\,\text{V}$, and frequency $f_s = 500$ Hz, applied directly across the VCM cell (red trace), and current flowing through it, for three tests, in which the device was preliminarily programmed into the first (blue trace), second (green trace), and third (magenta trace) resistance level in the set $R_0 \in \{910, 10800, 16600\}$ Ω. b) Time evolution of the trajectory point $(\tilde{v}_m(t), i_m(t))$ toward a unique pinched hysteresis loop, as extracted from each of the three experiments. In the indirect measurement of the core memristor voltage $\tilde{v}_m$, R_{contact} was estimated to be as large as 550 Ω. Arrows show how the core memristor current and voltage proceed as time goes by, over each input cycle, at steady state. Under each negative (positive) input half cycle, the most significant decrease (increase) in the core memristor resistance occurs along the locus branch indicated by the lowermost (uppermost) arrow with text label SET (RESET).

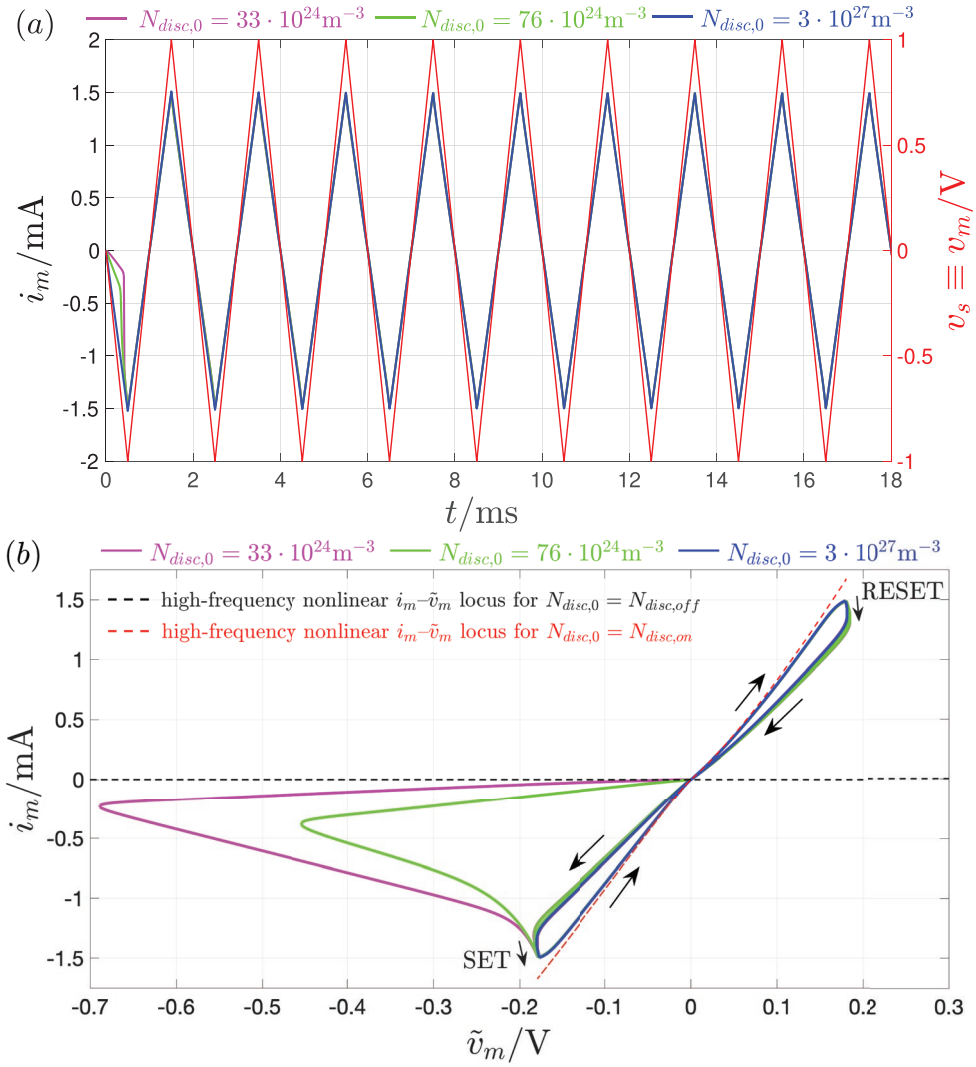


Figure 7. Capability of the JART VCM v1 model to capture the experimental observations from Figure 6. a) Time waveforms of the purely-AC periodic triangular voltage v_s of amplitude $\hat{v}_s = 1$ V, and frequency $f_s = 500$ Hz, applied between the ReRAM device terminals (red curve), and of the resulting cell current for the first (blue trace), second (green trace), and third (magenta trace) initial condition $N_{disc,\,0}$ in the set $\{3 \times 10^{27}, 76 \times 10^{24}, 33 \times 10^{24}\}\mathrm{m}^{-3}$. Note that the i^{th} initial condition in such a set corresponds to the ith resistance R_0 from the set {910, 10800, 16600} Ω, which was considered for the experiments resulting in the measurements illustrated in Figure 6 ($i \in \{1, 2, 3\}$). b) Core memristor current against core memristor voltage over the complete time duration of each of the three numerical simulations from plot (a). As in Figure 6, the core memristor voltage is calculated for a contact resistance $R_{contact}$ as large as 550 Ω. The clockwise direction of motion for the trajectory point $(\tilde{v}_m(t), i_m(t))$ on the unique pinched hysteresis loop, emerging after transients decay to zero, is clearly indicated with arrows. The RESET (SET) transition occurs in the first (third) quadrant of the $\tilde{v}_m$ versus i_m plane. The dashed black (red) single-valued curve represents the current– voltage characteristic of the core memristor, preliminary programmed into the lowest (highest) possible memory state $N_{disc,\,off}$ ($N_{disc,\,on}$), as observed in a model simulation under the application of a purely-AC periodic triangular voltage stimulus v_s, of amplitude $\hat{v}_s = 1.1$ V, and frequency $f_s = 22.72$ GHz across the VCM cell.

$\hat{v}_s = 1$ V and frequency $f_s = 500$ Hz across its terminals—refer to the red curve in plot (a) in either Figures 6 or 7—induces the emergence of history erase effects in the VCM cell, with the progressive evolution of its current toward a unique waveform, for each of the three initial conditions (the corresponding traces are differentiated through the use of different colors).

In all three experimental tests (numerical simulations), a unique pinched hysteresis loop appears, after transients fade away, in the plane, spanned by core memristor voltage $\tilde{v}_m$ and current i_m (refer to Figures 6b and 7b). The dashed black and red single-valued loci in Figure 7b represent the device response to a purely-AC periodic triangular voltage stimulus v_s of amplitude $\hat{v}_s = 1.1$ V and frequency $f_s = 22.72$ GHz, as observed in a simulation scenario, where the disc oxygen vacancy concentration was preliminarily initialized in the lowest $N_{disc,\,off}$ and highest $N_{disc,\,on}$ possible value in its admissible variation range. The input frequency in such a periodic stimulation test pair is too high to cause any noticeable modulation in the disc oxygen vacancy concentration per cycle, irrespective of the initial condition. Importantly, the unique current– voltage pinched hysteresis loop, which the core memristor exhibits under periodic stimulation at frequency f_s = 500 Hz, as inferable from the steady-state simulation results in

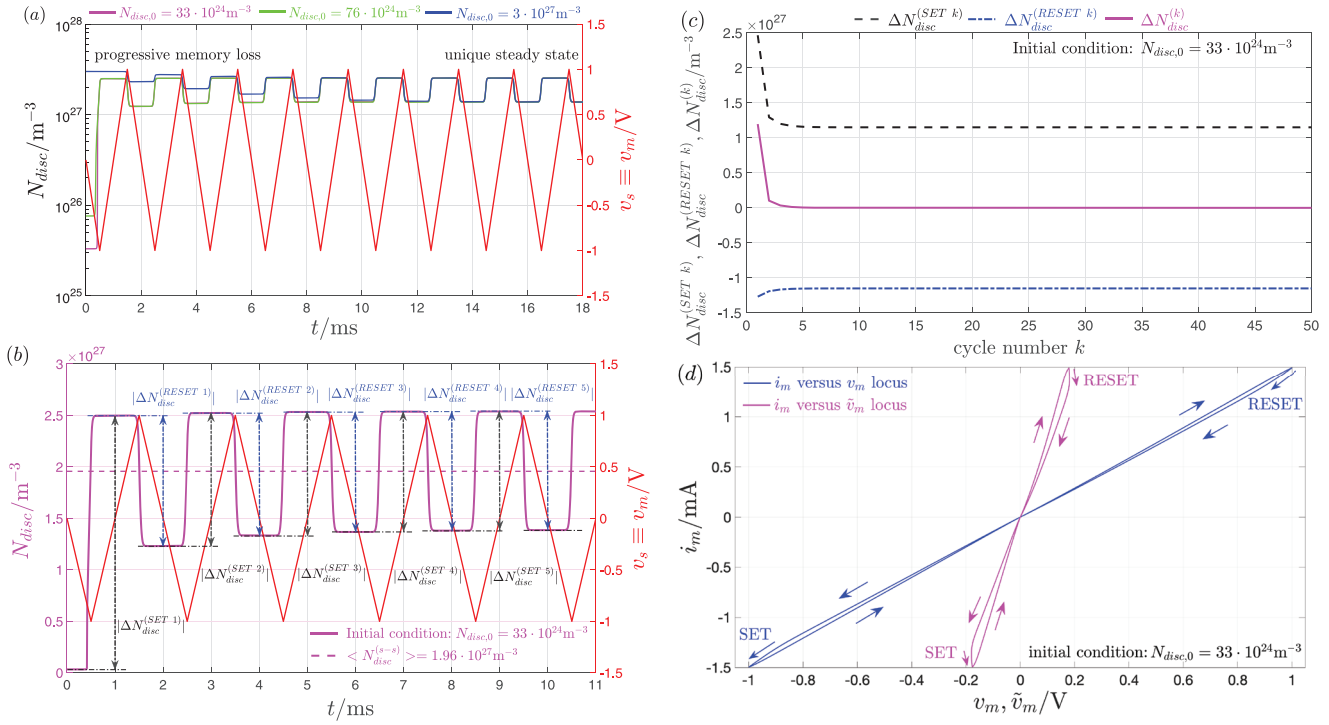


Figure 8. Evidence for the appearance of a unique steady state, independent of boundary effects, in response of the periodically-forced TaO_x ReRAM cell, as revealed by an insightful analysis of the numerical simulations of Figure 7. a) Disc oxygen vacancy concentration N_{disc} over time under the application of the voltage stimulus v_s (red curve) for the first (blue trace), second (green trace), and third (magenta trace) initial condition in the set $N_{disc,\,0} \in \{3 \times 10^{27}, 76 \times 10^{24}, 33 \times 10^{24}\}\mathrm{m}^{-3}$. Each trace converges asymptotically to an oscillatory solution $N_{disc}^{(s-s)}$, which is enclosed completely within the bounds of the memory state existence domain $\mathcal{D}$. b) Transitory behavior of the disc oxygen vacancy concentration N_{disc} from the lowest initial condition $N_{disc,\,0} = 33 \times 10^{24}\mathrm{m}^{-3}$ in the aforementioned set (magenta trace) toward the steady-state oscillatory waveform $N_{disc}^{(s-s)}$. The mean value $\langle N_{disc}^{(s-s)} \rangle$ of the steady-state oscillatory waveform $N_{disc}^{(s-s)}$ is found to be equal to $1.96 \times 10^{27}\ \mathrm{m}^{-3}$. The modulus of the positive (negative) change in the state $\Delta N_{disc}^{(\mathrm{SET}\,k)}$ ($\Delta N_{disc}^{(\mathrm{RESET}\,k)}$) over the negative (positive) half of the kth input cycle—$k \in \{1, 2, 3, 4, 5\}$ —is clearly indicated in black (blue). The level $\langle N_{disc}^{(s-s)} \rangle$, around which the disc oxygen vacancy concentration was found to oscillate at steady state, in this particular simulation,was computed across a time interval beyond the time frame visualized in this plot. c) Net memory state change $\Delta N_{disc}^{(k)} \triangleq \Delta N_{disc}^{(\mathrm{SET}\,k)} + \Delta N_{disc}^{(\mathrm{RESET}\,k)}$ (magenta trace) over the kth input cycle, and its two additive components, namely $\Delta N_{disc}^{(\mathrm{SET}\,k)}$ (dashed black trace) and $\Delta N_{disc}^{(\mathrm{RESET}\,k)}$ (dash-dotted blue trace), versus k, as extracted from plot (b). As transients fade away, the net change in the disc oxygen vacancy concentration per cycle vanishes, as expected. d) Blue (magenta) Lissajous curve: unique steady-state i_m versus v_m (i_m vs $\tilde{v}_m$) pinched hysteresis loop for the overall VCM cell (core memristor).

Figure 7a, lies entirely within the region comprised between the dashed black and red single-valued loci. Thus, boundary mechanisms have no impact on the emergence of fading memory effects in the VCM device in these circumstances. Moreover, it may be shown that, as the input frequency tends to infinity, the resistance of our core memristor depends upon its voltage, as expected of any resistance switching memory from the extended class.[8,55] However, since such a dependence becomes noticeable only under strong stimuli, it may not be appreciated by inspecting either of the black and red loci in Figure 7a.

Let us gain a deeper insight into the history loss phenomenon emerging in the periodically-forced ReRAM cell by analyzing in more detail the numerical simulations, which resulted in the data visualized in Figure 7. **Figure 8**a depicts in blue, green, and magenta the progressive approach of the disc oxygen vacancy concentration N_{disc} to a unique steady-state oscillatory solution from the first, second, and third initial condition in the set $N_{disc,\,0} \in \{3 \times 10^{27}, 76 \times 10^{24}, 33 \times 10^{24}\}\mathrm{m}^{-3}$, under the triangular voltage stimulus v_s shown in red. A close-up view of the transitory behavior of the memory state N_{disc} from one of these initial conditions, specifically $N_{disc,\,0} = 33 \times 10^{24}\ \mathrm{m}^{-3}$, which corresponds to a device resistance $R_0 = 16600\Omega$, is shown in plot (b) of the same figure (magenta trace) together with the input voltage (red trace). Before proceeding with the analysis of the simulation data, the following remark establishes a rigorous approach to derive the net change of the memory state over each cycle of the voltage stimulus.

Remark 2: Taking into account that for $t \in (0,\ T_s/2]$, with $T_s = 1/f_s$, the voltage stimulus v_s, depicted in red in Figure 8b, undergoes a negative excursion, inducing a SET transition in the ReRAM cell over the first half period, the increase (decrease) in the memory state over the first (second) half cycle of the kth input period is rigorously computable numerically via the first (second) equation in the set

$$\Delta N_{disc}^{(\mathrm{SET}\,k)} = \int_{t=(k-1)\cdot T_s}^{t=(k-1)\cdot T_s + T_s/2} \frac{\mathrm{d}N_{disc}}{\mathrm{d}t'}\,\mathrm{d}t' \quad \text{and} \tag{7}$$

$$\Delta N_{\text{disc}}^{(\text{RESET}\,k)} = \int_{t=(k-1)\cdot T_s+T_s/2}^{t=(k-1)\cdot T_s+T_s} \frac{\mathrm{d}N_{\text{disc}}}{\mathrm{d}t'}\,\mathrm{d}t'. \tag{8}$$

Computing the sum of the contributions in Equations (7) and (8) would then provide the net change $\Delta N_{\text{disc}}^{(k)}$ in the disc oxygen vacancy concentration over the k^{th} input cycle, that is,

$$\Delta N_{\text{disc}}^{(k)} = \Delta N_{\text{disc}}^{(\text{SET}\,k)} + \Delta N_{\text{disc}}^{(\text{RESET}\,k)}. \tag{9}$$

Naturally, in case $\Delta N_{\text{disc}}^{(k)}$ were found to be positive (negative), one would conclude that the SET (RESET) forces win over the RESET (SET) ones across the k^{th} input cycle.

In the simulation scenario under focus, the increase (decrease) in memory state over the kth negative (positive) half-cycle of the voltage stimulus results in a positive (negative) change $\Delta N_{\text{disc}}^{(\text{SET}\,k)}$ ($\Delta N_{\text{disc}}^{(\text{RESET}\,k)}$) in N_{disc} during the kth input period, as clearly marked in Figure 8b for $k \in \{1, 2, 3, 4, 5\}$. The net memory state change over the kth cycle of the input voltage, computable via $\Delta N_{\text{disc}}^{(k)} = \Delta N_{\text{disc}}^{(\text{SET}\,k)} + \Delta N_{\text{disc}}^{(\text{RESET}\,k)}$, is found to reduce progressively with k, converging toward zero asymptotically (refer to Figure 8c). This reveals that, *at steady-state, the counteractive SET and RESET forces balance out*. Importantly, referring to Figure 8b, at steady state, the disc oxygen vacancy concentration N_{disc} is found to settle on a periodic oscillatory solution $N_{\text{disc}}^{(\text{s-s})}$, which is centered around a mean value $\langle N_{\text{disc}}^{(\text{s-s})} \rangle$ of 1.96×10^{27} m^{-3}. This value lies entirely within the memory state allowable existence domain $\mathcal{D}$, which confirms that, in this scenario, *boundary effects have no impact on the unique steady-state response of the periodically-forced ReRAM cell*. Furthermore, Figure 8d compares the pinched hysteresis loop, observed at steady state in the voltage versus current plane of the core memristor (magenta trace) to the corresponding locus, appearing in the voltage versus current plane of the overall VCM cell (blue trace), which reveals the significant impact of the series resistance R_{contact} on the voltage dropping across the core memristor, after transients vanish, in this scenario.

5. System-Theoretic Exploration of the History Erase Effects under Periodic Forcing

As a preliminary step toward the exploration of the AC response of the VCM cell, the next section introduces and discusses its DRM on the basis of the first-order JART VCM v1 model. The concept of the DRM is defined in Section S3, Supporting Information.

5.1. DRM of the ReRAM Device

The DRM of the ReRAM cell consists of the combination of the two families of SET and RESET SDRs, in turn referred to as SET and RESET DRMs, which denote an ensemble of $|\mathrm{d}N_{\text{disc}}/\mathrm{d}t|$ versus N_{disc} loci, parameterized by a negative-valued and a positive-valued bias voltage V_{m}, let fall across the physical stack, respectively. **Figure 9** illustrates 11 paired SET and RESET SDRs from the DRM of the ReRAM cell under the assumption that R_{contact} amounts to 550 Ω. The solid (dashed) arrowed trace in the ith pair of SDRs, sharing a common color, as indicated in the legend, and denoting a particular SET (RESET) SDR, specifies the path, which the disc oxygen vacancy concentration N_{disc} is bound to follow over time as it increases (decreases) under a negative (positive) DC voltage V_{m} of modulus $|V_{\text{m}}| = V_{\text{m}}^{*}$ equal to the ith element in the set {0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.6, 0.7, 0.8, 0.9, 1.0, 1.1} V. As expected from the study in Section 3, the continuous application of a negative (positive) bias voltage across the VCM cell induces its progressive SET (RESET) switching transition, which results in the asymptotic convergence of the disc oxygen vacancy concentration N_{disc} to its highest (lowest) possible value $N_{\text{disc, on}}$ ($N_{\text{disc, off}}$). In order to capture the clipping effect, which the memory state N_{disc} eventually experiences, as it attains the upper (lower) bound in its existence domain $\mathcal{D}$ under any negative (positive) DC stimulus, the JART VCM v1 model is endowed with ad hoc boundary conditions. These boundary conditions impose that, if, at any time, N_{disc} increases up to $N_{\text{disc, on}}$ (decreases down to $N_{\text{disc, off}}$) under any negative-valued (positive-valued) DC input, then $\mathrm{d}N_{\text{disc}}/\mathrm{d}t$ instantaneously drops to zero, keeping null thereafter, unless the sign of the stimulus is reversed. In order to reveal the multi-decade variation in the device switching rate $\mathrm{d}N_{\text{disc}}/\mathrm{d}t$, which emerges, in general, under any given DC voltage stimulus across the admissible memory state existence domain $\mathcal{D}$, a logarithmic scale was adopted in Figure 9 to report values along the vertical axis. As a result, the location of the equilibrium of the state Equation (1), as introduced by the SET (RESET) boundary condition, at $N_{\text{disc}} = N_{\text{disc, on}}$ ($N_{\text{disc}} = N_{\text{disc, off}}$) for each negative (positive) V_{m} value, may not be marked on this graphical illustration. For the same reason, the power-off plot (POP), referable either as the SET or as the RESET SDR for zero input, which, employing a linear scale for the $|\mathrm{d}N_{\text{disc}}/\mathrm{d}t|$ axis, would appear as a line of equilibria, sitting along the N_{disc} axis throughout the memory state existence domain $\mathcal{D}$, and revealing the analogue non-volatile memory capability of the VCM cell, may not be drawn in Figure 9.

At each point $P = (N_{\text{disc}}, |\mathrm{d}N_{\text{disc}}/\mathrm{d}t|)$ on a given SET or RESET SDR, the time scale τ of the ReRAM device response to the associated DC voltage stimulus at the time, when the memory state attains the value expressed by the abscissa of the point itself, may be estimated simply as

$$\tau = \frac{N_{\text{disc}}}{|\mathrm{d}N_{\text{disc}}/\mathrm{d}t|} \tag{10}$$

Endowing the log– log DRM of the ReRAM cell with a dense family of parallel lines, parametrized by a control coefficient, namely the time scale τ, and defining functions of the form

$$\log_{10}|\mathrm{d}N_{\text{disc}}/\mathrm{d}t| = \log_{10} N_{\text{disc}} + \log_{10}\frac{1}{\tau} \tag{11}$$

may allow to estimate, by visual inspection, how many orders of magnitude in time scale does the switching transition of the DC-driven VCM cell evolves along. The set of black dashed lines, depicted in Figure 9, as extracted from Equation (11) for $\tau \in$ {1 ns, 1 µs, 1 ms, 1 s, 1 ks, 1 ms, 1 Gs, 1 Ts}, provide information on the multi-scale timing of the response of the ReRAM device to any given bias voltage stimulus. In fact, an order of magnitude for the time scale of the response of the ReRAM

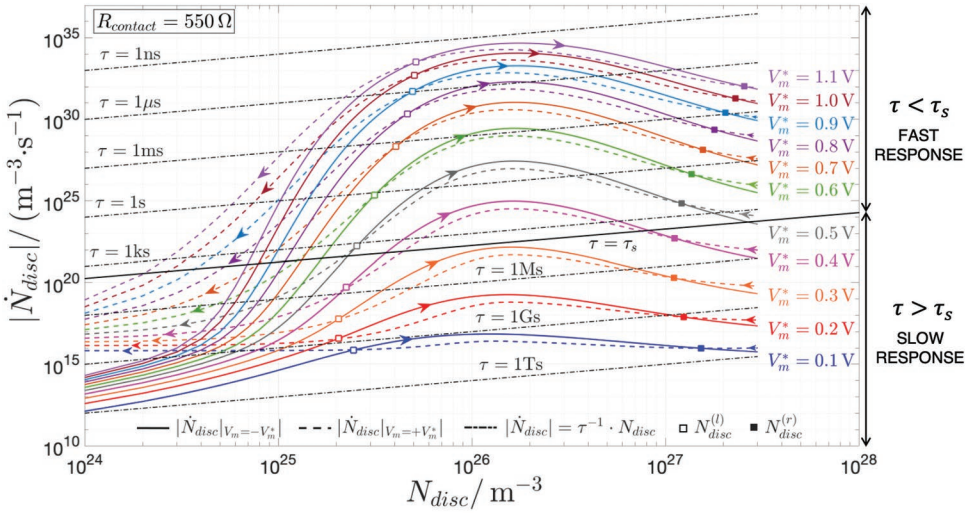


Figure 9. Family of arrowed $|\dot{N}_{disc}| \triangleq |dN_{disc}/dt|$ versus N_{disc} loci forming the DRM of the TaO_x ReRAM cell, according to the JART VCM v1 model, for $R_{contact} = 550\ \Omega$, in log– log scale. In each pair of arrowed loci, sharing the same color, as indicated in the legend, the dashed RESET (solid SET) SDR indicates the modulation in the negative-valued (positive-valued) switching transition rate dN_{disc}/dt, as the memory state N_{disc} decreases (increases) over time from a certain initial condition $N_{disc,\,0}$ under the application of a positive (negative) DC voltage $V_m = +(-)V_m^*$, of fixed modulus $|V_m| = V_m^*$, across the physical stack. The family of black dashed parallel log– log loci, parametrized by the time scale τ, as indicated in Equation (11), form the memristor response timing diagram, which allows to infer visually the spread in time scale in the device response to a given bias voltage, let fall across the physical stack, by simply recording the label of the linear locus at closer distance to the running trajectory point $P = (N_{disc}, |dN_{disc}/dt|)$, at any time throughout the DC stress test. The memristor response timing diagram can be used also to monitor the multi-decade variation in time scale in the device dynamics under periodic stimulation, but this requires to update the RESET (SET) SDR, along which the trajectory point lies at any given time, depending upon the running positive (negative) stimulus value, before reading the label of the linear locus at closer distance from the current trajectory point itself. Importantly, whether, at any given time, the device dynamics, induced by the application of a periodic stimulus across the physical stack, appear slow or fast, to the eyes of an external observer, depends critically upon the ratio between the memristor response time scale τ, and the fixed input signal time scale τ_s, which is estimated from the excitation frequency s_s via Equation (12). If, at any given time, the trajectory point $P = (N_{disc}, |dN_{disc}/dt|)$ visits the plane region of the DRM plane, located below (above) the black solid log– log linear locus, extracted from the family of functions in Equation (11) for $\tau = \tau_s$, and representing the input timing diagram, the further away from the same line were the running trajectory point located, and the slower (faster) would the device kinetics appear, to an external observer, relative to the input dynamics. Each pair of RESET and SET SDRs cross twice, one with the other, over the memory state existence domain $\mathcal{D}$ (refer to the hollow and filled square markers, indicating the positions of the left and right intersections, named $N_{disc}^{(l)}$ and $N_{disc}^{(r)}$, respectively). The right crossing between the RESET and SET SDRs in a given pair, identifiable with a certain label V_m^*, is found to approximate rather well the time average of the steady-state oscillation, observed in the memory state, as a result of fading memory effects, which emerge, during transients, in the ReRAM cell, upon its excitation through a purely-AC periodic voltage stimulus v_s of amplitude $\hat{v}_s = V_m^*$. The accuracy of the approximation improves under appropriate choices for the excitation frequency f_s (refer to Remark 4).

cell to a certain DC input at any point in time may be quickly inferred by reading the parameter, labeling the black dashed line at closer distance from the point P, sitting along the relevant SDR, and featuring as abscissa the memory state value at the given time. For this reason, the family of linear loci, defined in Equation (11), is referred to as *memristor response timing diagram* in the remainder of the paper. Since a larger (smaller) vertical shift for a line in the family from Equation (11) indicates a shorter (longer) time scale τ in the memristor response, as, under a specific negative or positive DC stimulus, the trajectory point $P = (N_{disc}, |dN_{disc}/dt|)$ travels toward (away from) the hump of the respective SET or RESET SDR, the switching transition of the ReRAM device gains (loses) speed, confirming the investigations from Section 3.

5.2. Analysis of the AC Response of the ReRAM Cell

The investigation of the resistance switching phenomena, emerging in the VCM cell, under the application of a periodic voltage stimulus v_s with zero mean across its terminals, is certainly way more complicated than the analysis of the device response under DC excitation. As a purely-AC voltage stimulus assumes progressively all values in the range $[-\hat{v}_s, \hat{v}_s]$, where $\hat{v}_s$ denotes the input amplitude, the trajectory point in the $|dN_{disc}/dt|$ versus N_{disc} plane evolves continuously across each of the SET/RESET SDRs associated to negative/positive V_m values within the same range, twice over each period. With this in mind, the time scale, along which the response of the periodically-driven VCM cell evolves at any time, may be computed via Equation (10), or estimated by graphical inspection through the support of the memristor response timing diagram, once the memory state N_{disc} and stimulus value v_s at the given time are known, which unequivocally defines the present location of the point P on the $|dN_{disc}/dt|$ versus N_{disc} plane. As clarified in the analysis of the device response to DC stress tests, whether, in a practical experiment, the dynamics of the periodically-driven device appears slow or fast at any given time over each input cycle does not depend merely upon this absolute time scale measure. The following remark, which is the variant of Remark 1 from Section 3 for purely-AC periodic device stimulation tests, clarifies this important aspect.

Remark 3: Applying a purely-AC periodic voltage stimulus of amplitude $\hat{v}_s$ and frequency f_s across the ReRAM cell, whether, at any given time, the device dynamics would appear slow or fast, to the eyes of an external observer, depends crucially upon the ratio between the present device response time scale τ and the fixed input time scale τ_s, which characterizes the evolution of the excitation signal, and may be estimated as

$$\tau_s = \frac{1}{f_s} \tag{12}$$

In fact, at any given time, the larger (smaller) the time scale ratio τ/τ_s is, relative to unity, the slower (faster) would the motion of the memory state appear, in comparison to the concurrent variation in the periodic stimulus.

Let us now assume to apply a purely-AC periodic voltage stimulus v_s of amplitude $\hat{v}_s$ and frequency f_s between the terminals of the ReRAM cell. In order to acquire some insightful indication on the alternating slow/fast dynamics of the device response over each input cycle, on the basis of Remark 3, it is beneficial to draw yet another linear locus on the VCM cell DRM, already augmented with the memristor response timing diagram (recall Figure 9). This new line is defined as the graph of a log– log function, extracted from the family of Equation (11) for $\tau = \tau_s$, with τ_s computed via Equation (12). Since this linear locus clearly indicates the fixed time scale, along which the stimulus evolves over time, it is referred to as *input timing diagram* in the remainder of this manuscript. Thus, when employing a graphical inspection approach, at any given time, during the periodic excitation of the VCM cell, the further below (above) the input timing diagram, for example, the black dashed line in Figure 9, were the trajectory point P found on the $|dN_{disc}/dt|$ versus N_{disc} plane, and the slower (faster) would the resulting memory state motion appear, to an external observer.

In order to provide clear evidence for the soundness of this theoretical analysis, let us process the data extracted from the numerical simulation of Figure 8b. **Figure 10** shows the time series of the signed time derivative of the disc oxygen vacancy concentration against the time series of the disc oxygen vacancy concentration

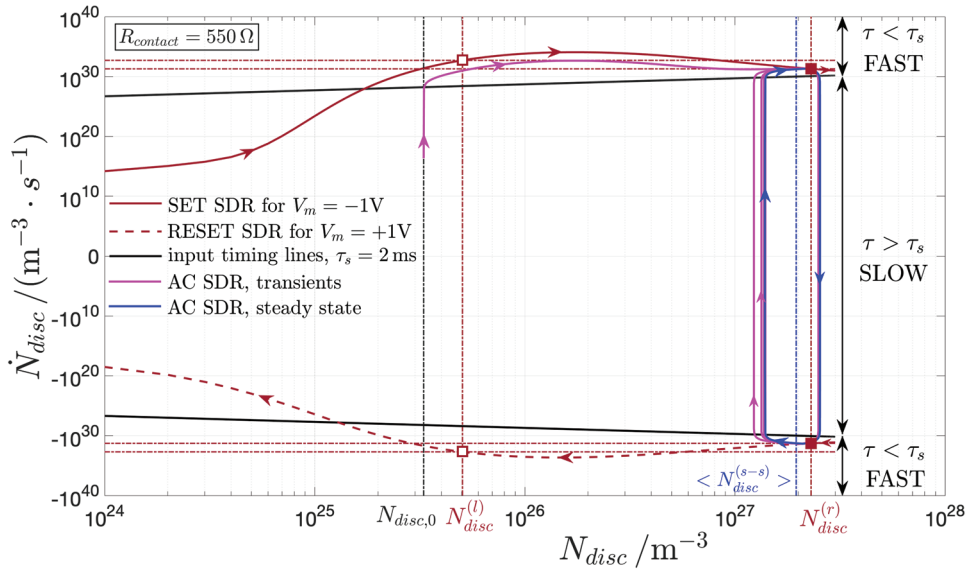


Figure 10. Transients (magenta branch) and steady state (blue branch) in the time course of the $\dot{N}_{disc} \triangleq dN_{disc}/dt$ versus N_{disc} log– log locus, showing an AC SDR of the ReRAM cell, as it results from a JART VCM v1 model numerical simulation, in which a purely-AC periodic triangular voltage signal v_s, of amplitude $\hat{v}_s = 1$ V and frequency $f_s = 500$ Hz, is applied across the physical stack, preliminarily programmed into a resistance state corresponding to the initial condition $N_{disc,0} = 33 \times 10^{24}\mathrm{m}^{-3}$ (refer to the simulation of Figure 8b). During the positive (negative) excursion of the voltage stimulus, and twice over each cycle, the trajectory point $P = (N_{disc}, dN_{disc}/dt)$ travels across a continuum of RESET (SET) SDRs, namely all those associated to DC voltages, let fall across the ReRAM cell, in the range $(0,\hat{v}_s]$ ($[-\hat{v}_s,0)$). Due to the asymmetry between the RESET and SET switching kinetics of the VCM cell, over any period of the voltage stimulus, during the transient phase, the spread in time scale in the device dynamics differs over the positive and negative input half cycles, respectively. As a result, since, at any given time, during the positive (negative) excursion of the voltage stimulus, it is the ratio between the present memristor RESET (SET) response time scale τ and the fixed input time scale τ_s, that is, the location of the current trajectory point relative to the lower (upper) black solid positive (negative) input timing line, which dictates whether, practically, the off (on) switching transition is slow or fast, as well as how slow or fast is, clearly, throughout the transient phase, some imbalance between the effects of the RESET and SET forces on the device dynamics will induce a net change in its memory state, over each cycle. In the simulation scenario under focus, the SET forces prevail over the RESET ones, cycle after cycle, over the transient phase, and, eventually, the memory state is found to revolve periodically around the blue closed orbit, as expected, given that the device displays an oscillatory behavior at steady state (see Figure 8b). Very interestingly, the mean value $\left\langle N_{disc}^{(s-s)} \right\rangle = 1.96 \times 10^{27}$ m^{-3} of the oscillatory signal $N_{disc}^{(s-s)}$, defining the time evolution of the disc oxygen vacancy concentration at steady state, is found to be approximated rather well by the right crossing $N_{disc}^{(r)} = 2.30 \times 10^{27}$ m^{-3} between the brown dashed RESET and solid SET SDRs from the DRM of Figure 9, respectively associated to a positive and negative DC voltage V_m of modulus V_m^* equal to the amplitude $\hat{v}_s$ of the excitation signal v_s, let fall across the physical stack. It is important to observe that the brown hollow (filled) square on the left (right) crossing between the RESET and SET SDRs from the DRM of Figure 9 appears as a pair of identical markers, featuring the same abscissa but opposite ordinates, in this illustration, where, as remarked earlier, the polarity of the switching speed is accounted for, along the vertical axis.

itself, over the entire simulation time. The resulting locus of points, representing what we refer to as an *AC state dynamic route* (AC SDR), depicted in magenta, over the transient phase, and in blue, at steady state, allows to visualize the time evolution of the memory state, over the positive (negative) excursion of the voltage stimulus in each cycle, within the lower (upper) half plane. Additionally, accounting not only for the modulus but also for the sign of $\mathrm{d}N_{\mathrm{disc}}/\mathrm{d}t$, in reporting values along the vertical axis of the plane, displaying N_{disc} on the horizontal axis, requires to split the memristor response timing diagram into two sub-diagrams. The one for the RESET transition is located in the lower half plane. It consists of the family of memristor response RESET timing lines, mathematically described via

$$\log_{10}\left|\mathrm{d}N_{\mathrm{disc}}/\mathrm{d}t\right| = -\log_{10} N_{\mathrm{disc}} - \log_{10}\frac{1}{\tau} \tag{13}$$

On the other hand, the sub-diagram for the SET transition is located in the upper half plane. It is composed of the family of memristor response SET timing lines, mathematically expressed by

$$\log_{10}\mathrm{d}N_{\mathrm{disc}}/\mathrm{d}t = \log_{10} N_{\mathrm{disc}} + \log_{10}\frac{1}{\tau} \tag{14}$$

As a further consequence of reporting signed values for the switching transition rate on the vertical axis of the plane, featuring the memory state on the horizontal axis, the input timing diagram also bifurcates into a couple of linear loci, referred to as positive and negative input timing lines. These lines are extracted from the families in Equations (13) and (14), respectively, for $\tau = \tau_{\mathrm{s}}$.

With reference to Figure 10, a point $P = (N_{\mathrm{disc}}, \mathrm{d}N_{\mathrm{disc}}/\mathrm{d}t)$, progresses toward the west (east) over the positive (negative) excursion of the periodic voltage stimulus in each cycle, as it draws either the magenta or the blue branch of the AC SDR over the transient and steady-state phase, respectively. Very importantly, over any time interval, when this point visits the area enclosed within the two black solid positive and negative input timing lines, the path, it draws, stretches mostly along the vertical direction. This reveals a negligible change in the memory state, in line with the predictions drawn earlier from the system-theoretic analysis. On the other hand, during any time interval, when this point visits the plane region below (above) the positive (negative) input timing line, the route, it follows, extends alongside the RESET (SET) SDR, which dictates the memory state evolution under a positive (negative) bias voltage $V_{\mathrm{m}} = +(-)V_{\mathrm{m}}^{*}$, of modulus $V_{\mathrm{m}}^{*} = \hat{v}_{\mathrm{s}} = 1$ V. This reveals a noticeable change in the memory state, confirming the insights gained beforehand by means of system-theoretic investigations. Moreover, starting from the initial condition $N_{\mathrm{disc,\,0}} = 33 \times 10^{24}$ m^{-3}, the trajectory point $P = (N_{\mathrm{disc}}, \mathrm{d}N_{\mathrm{disc}}/\mathrm{d}t)$ first undergoes a net eastward motion from cycle to cycle, indicating that the SET forces dominate over the RESET ones, throughout the transient phase. At some point in time, however, the effects of the counteractive RESET and SET resistance switching transition mechanisms balance out. This results in the periodic revolution of the trajectory point along the blue closed orbit throughout the steady-state phase, over each input cycle.

Let us now focus on the implications of the fading memory effects, which accompany the resistance switching phenomena, emerging in the periodically-forced physical stack, on its steady-state behavior. With reference to Figure 10, the two brown dashed and solid arrowed curves respectively represent the RESET and SET SDRs of the VCM cell for a positive-valued and negative-valued DC voltage V_{m}, let fall across the ReRAM device, of modulus V_{m}^{*} equal to the periodic stimulus amplitude $\hat{v}_{\mathrm{s}}$, set to 1 V in the simulation of Figure 8b. This pair of RESET and SET SDRs admit two crossing points, namely $N_{\mathrm{disc}} = N_{\mathrm{disc}}^{(\mathrm{l})} = 5.05\times10^{25}$ m^{-3}, and $N_{\mathrm{disc}} = N_{\mathrm{disc}}^{(\mathrm{r})} = 2.30\times10^{27}$ m^{-3}, at which

$$\left|\mathrm{d}N_{\mathrm{disc}}/\mathrm{d}t\right|_{V_{\mathrm{m}}=+V_{\mathrm{m}}^{*}} = \left|\mathrm{d}N_{\mathrm{disc}}/\mathrm{d}t\right|_{V_{\mathrm{m}}=-V_{\mathrm{m}}^{*}} \tag{15}$$

This may be evinced also by inspecting this very same SDR pair in the ReRAM cell DRM of Figure 9. With reference to the blue orbit in Figure 10, that is, to the steady-state branch of the AC SDR, resulting from the simulation of Figure 8b, the mean value $\left\langle N_{\mathrm{disc}}^{(s-s)}\right\rangle = 1.96\times10^{27}$ m^{-3} of the steady-state oscillatory waveform $N_{\mathrm{disc}}^{(s-s)}$ of the disc oxygen vacancy concentration is found to be impressively close to the abscissa of the right intersection $N_{\mathrm{disc}}^{(\mathrm{r})} = 2.30\times10^{27}$ m^{-3} between the aforementioned paired RESET and SET SDRs. In general, this crossing point is not expected to define rigorously the level, around which, asymptotically, the memory state solution is found to oscillate. First, because the DRM does not constitute the appropriate tool to investigate the dynamics of a periodically-driven system. Second, because the input signal assumes all values in the range $[-\hat{v}_{\mathrm{s}}, \hat{v}_{\mathrm{s}}]$, twice over each period, while $N_{\mathrm{disc}}^{(\mathrm{r})}$ merely corresponds to the right intersection between the paired RESET and SET SDRs, referring to the case, where the device voltage is fixed to the absolute maximum and minimum of the input signal, respectively. This notwithstanding, the proximity between $\left\langle N_{\mathrm{disc}}^{(s-s)}\right\rangle$ and $N_{\mathrm{disc}}^{(\mathrm{r})}$, in the scenario under focus, is worth of a deeper investigation. In fact, with reference to the case study, illustrated in Figure 10, in view of the intrinsic variability in the electrical behavior, characterizing a periodically-driven ReRAM cell, cycle after cycle, $N_{\mathrm{disc}}^{(\mathrm{r})}$ represents a rather good approximation for the time average of the oscillation in the disc oxygen vacancy concentration, at steady state. The following remark explains why, in general, the accuracy of an approximation of this kind depends critically upon the excitation frequency f_{s}.

Remark 4: Looking at Figure 9, and comparing the strengths of the RESET and SET switching transition rates, that is, respectively, $\left|\mathrm{d}N_{\mathrm{disc}}/\mathrm{d}t\right|_{V_{\mathrm{m}}=V_{\mathrm{m}}^{*}}$ and $\left|\mathrm{d}N_{\mathrm{disc}}/\mathrm{d}t\right|_{V_{\mathrm{m}}=-V_{\mathrm{m}}^{*}}$, for a given RESET and SET SDR pair with label V_{m}^{*}, in the neighborhood of the respective left (right) crossing $N_{\mathrm{disc}}^{(\mathrm{l})}$ ($N_{\mathrm{disc}}^{(\mathrm{r})}$), it is clear that the RESET (SET) forces are dominant over the SET (RESET) ones on its left, while the SET (RESET) forces win over the RESET (SET) ones on its right. As a result, the competition between the RESET and SET switching mechanisms, over each cycle of a hypothetical symmetric square wave voltage stimulus v_{s} of amplitude $\hat{v}_{\mathrm{s}} = V_{\mathrm{m}}^{*}$, let fall across the ReRAM cell, would inevitably result in the progressive motion of the memory state, initiated in the neighborhood of the left (right) crossing $N_{\mathrm{disc}}^{(\mathrm{l})}$ ($N_{\mathrm{disc}}^{(\mathrm{r})}$), away from (toward) it.

In fact, this holds true also upon stimulating the device with a purely-AC periodic triangular voltage signal v_s of the same amplitude, under excitation frequency choices, ensuring that the memory state keeps practically motionless until (undergoes a noticeable change only when) the modulus of the input signal approaches its peak value.

Upon setting the excitation frequency f_s of the triangular voltage stimulus v_s, of unitary amplitude $\hat{v}_s$, to 500 Hz, for the simulation of Figure 8b, the right crossing point of the RESET and SET SDR pair, identifiable through the label $V_m^* = 1$ V, provides a rather accurate approximation for the mean value of the steady-state oscillation in the memory state (refer to Figure 10). However, on the basis of Remark 4, this approximation may be improved, upon increasing the input frequency to the point, when, ideally, under the positive (negative) excursion of the voltage stimulus over each cycle, the device state keeps approximately motionless unless the input signal attains its absolute maximum (minimum) value, which would make the dashed (solid) brown RESET (SET) SDR in Figure 10 the only possible path, along which decremental (incremental) changes in the disc oxygen vacancy concentration may ever occur during the RESET (SET) transition phase. Repeating the simulation from Figure 8b for a number of higher values assigned to the excitation frequency f_s, namely each one in the set {1.5, 5, 15} kHz, and initializing the memory state N_{disc} in either of two distinct values, specifically $N_{disc,\,0} = 76 \times 10^{24}$ m^{-3} and $N_{disc,\,0} = 3 \times 10^{27}$ m^{-3}, sitting, respectively, to the left and to the right of the right crossing $N_{disc}^{(r)} = 2.30 \times 10^{27}$ m^{-3} between the brown dashed RESET and solid SET SDRs from Figure 10, the time course of the numerical solution to the JART VCM v1 model, for each simulation scenario, is illustrated in **Figure 11**, where the result, pertaining to the original case study, with the excitation frequency set to 500 Hz, is also reported for reference. The asymptotic convergence of the pair of traces, associated to any given input frequency choice, to the same oscillatory solution provides further evidence for the fading memory effects, emerging in the periodically-driven ReRAM cell. Most importantly, as the excitation frequency is increased over the range of values under consideration, the right crossing $N_{disc}^{(r)}$ between the brown dashed RESET and solid SET SDRs with label $V_m^* = 1$ V from Figure 9—refer to the brown-filled square marker in the same figure—is found to approximate better and better the mean value $\langle N_{disc}^{(s-s)} \rangle$ of the steady-state oscillatory waveform $N_{disc}^{(s-s)}$ of the disc oxygen vacancy concentration, under the application of a purely-AC periodic triangular voltage signal of amplitude $\hat{v}_s = V_m^* = 1$ V. This confirms the predictive power of the system-theoretic analysis outlined in Remark 4. Another aspect of interest, which this numerical investigation unveils, is the monotonic decrease in the amplitude of the steady-state oscillation in the memory state with the excitation frequency, which is expected of any periodically-driven memristor.[55]

Next, a sweep analysis, varying the peak voltage $\hat{v}_s$ of the stimulus from Figure 8b, was carried out, so as to investigate whether, for each simulation scenario, the mean value of the steady-state oscillation in the memory state response would be approximated satisfactorily well by the right crossing between the relevant pair of RESET and SET SDRs from the VCM cell DRM of Figure 9. For this purpose, the ReRAM device was driven by a purely-AC periodic triangular voltage stimulus v_s, with an amplitude $\hat{v}_s$, stepped across the set {0.1, 0.2, 0.3, 0.4, 0., 0.6, 0.7, 0.8, 0.9, 1, 1.1} V, and a frequency f_s, adapted to the input amplitude itself, in each test, as described shortly (see Remark 5), for either of two distinct initial conditions, namely $N_{disc,\,0} = 1 \times 10^{26}$ m^{-3}, and $N_{disc,\,0} = 3 \times 10^{27}$ m^{-3}, respectively

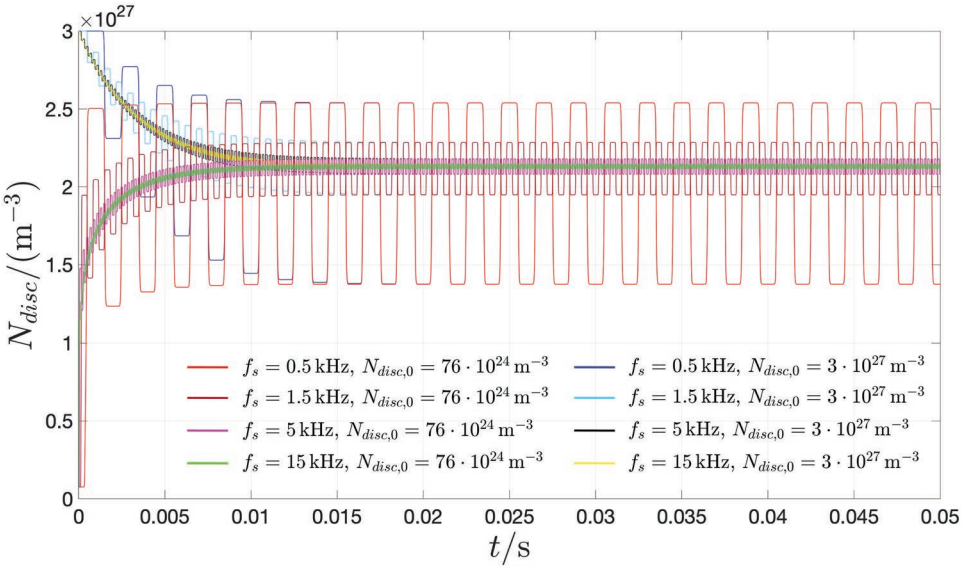


Figure 11. Time evolution of the memory state N_{disc} under the application of a purely-AC periodic triangular voltage stimulus v_s of amplitude $\hat{v}_s = 1$ V and each frequency f_s within the set {0.5, 1.5, 5, 15} kHz, from either of two different initial conditions, namely $N_{disc,\,0} = 76 \times 10^{24}$ m^{-3}, and $N_{disc,\,0} = 3 \times 10^{27}$ m^{-3}, respectively lying to the left and to the right of the right crossing point $N_{disc}^{(r)} = 2.30 \times 10^{27}$ m^{-3} between the brown dashed RESET and solid SET SDRs from Figure 10. The observations clearly reveal the fading memory of the periodically-driven VCM cell. Furthermore, and most importantly, as the excitation frequency increases, the mean value of the resulting steady-state oscillation in the memory state is approximated better and better by the right crossing $N_{disc}^{(r)}$ between the aforementioned RESET and SET SDRs, in line with the system-theoretic analysis from Remark 4.

lying to the left and to the right of the right crossing point between the respective paired RESET and SET SDRs, with label $V_m^* = \hat{v}_s$, from the ReRAM cell DRM of Figure 9.

Remark 5: As mentioned in the discussion of the simulation results from Figure 11, increasing the excitation frequency f_s, so as to activate the memristor dynamics only when the voltage stimulus v_s approaches its peak value $\hat{v}_s$, may allow to improve the prediction of the mean value $\langle N_{disc}^{(s-s)} \rangle$ of the steady-state oscillation $N_{disc}^{(s-s)}$ in the disc oxygen vacancy concentration under periodic stimulation of the VCM cell. However, the frequency cannot be increased arbitrarily, but should rather be adapted to the amplitude v_s of the voltage stimulus. In fact, in principle, applying a purely-AC periodic triangular voltage stimulus v_s of given amplitude $\hat{v}_s$ for a suitable initial condition, transients will eventually decay to zero, and the memory state would be found to evolve along a stable oscillatory waveform at steady state, irrespective of the excitation frequency. However, if the value assigned to f_s were too large, for example, if, with reference to the ReRAM cell DRM from Figure 9, the black dashed log– log line lay entirely above the SDR pair, identifiable with the label $V_m^* = \hat{v}_s$, then, depending upon the vertical shift in the input timing diagram, many thousands, millions, or even billions of input cycles might be necessary for the transients to vanish. Under circumstances of this kind, the resulting extremely-long simulation times would require the availability of an immense data storage unit to save the numerical data with a sufficiently-good time resolution. This issue stems from the impressively-high nonlinearity of the switching kinetics of the ReRAM device, as beautifully illustrated by the cell DRM of Figure 9, as extracted from the JART VCM v1 model. In fact, since the memristor response time scale τ varies over a huge number of decades across the DRM plane from this figure, the excitation frequency f_s has a major impact on the duration of the transient phase in the time evolution of the memory state of the periodically-driven ReRAM cell, together with other two important factors, specifically the input amplitude $\hat{v}_s$, and the initial condition $N_{disc,0}$.

In order to favor the emergence of a steady state, in each numerical simulation from the sweep analysis, within 10–100 input cycles, the excitation frequency f_s was chosen approximately as the inverse of the memristor response time scale τ at the right crossing $N_{disc}^{(r)}$ between the pair of RESET and SET SDRs with label V_m^* equal to the relevant value of the variable parameter $\hat{v}_s$ under variation. Importantly, for the lower input amplitude values in the set, considered for the sweep analysis of **Figure 12**, the proposed rule of thumb leads to the selection of excitation frequencies, corresponding to huge time scales, of no practical relevance. This shows that the effects of the fading memory of the ReRAM cell on its steady-state behavior under periodic forcing may be recorded, within reasonable times, in a laboratory experiment, only for specific input settings. Ad hoc stack engineering optimizations could be worked out, in the years to come, so as to modulate the families of RESET and SET SDRs for widening the input parameter domain, which induces the emergence of practically-exploitable history erase effects in the ReRAM cell (see Figure 14 for a hint on possible future research investigations).

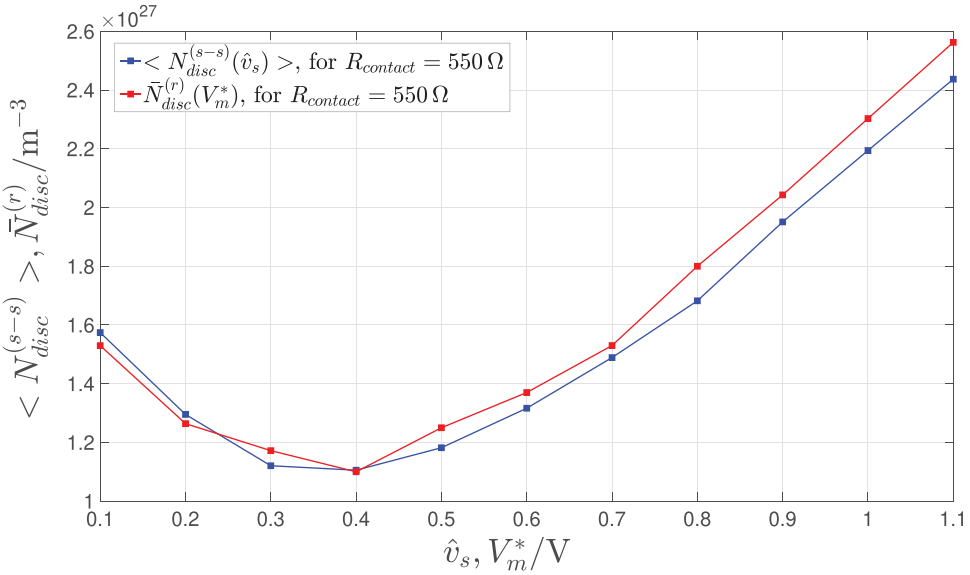


Figure 12. Blue trace: Time average $\langle N_{disc}^{(s-s)} \rangle$ of the steady-state oscillatory solution $N_{disc}^{(s-s)}$ of the state Equation (1) versus peak value $\hat{v}_s$ of the purely-AC periodic triangular voltage stimulus v_s, assumed to fall across the ReRAM cell, during the numerical simulation. For each input peak value scenario, the initial condition $N_{disc,0}$ was set to either of two values, specifically $\{1 \times 10^{26}, 3 \times 10^{27}\}$ m^{-3}, so as to ascertain the approach of the memory state to the same asymptotic waveform from starting points lying below and above the steady-state oscillation, as resulting from the fading memory of the ReRAM device. The excitation frequency f_s was reprogrammed for each input peak value case, according to the rule of thumb defined in Remark 5. The ith value in the set $\{3.75 \times 10^{-12}, 1.88 \times 10^{-10}, 3.33 \times 10^{-8}, 7.5 \times 10^{-6}, 0.75 \times 10^{-3}, 3.58 \times 10^{-2}, 8.21 \times 10^{-1}, 10, 8.33 \times 10^{2}, 7.50 \times 10^{3}, 6.82 \times 10^{4}\}$Hz was assigned to the excitation frequency f_s in the test, where the stimulus peak value $\hat{v}_s$ was chosen as the ith element from the list {0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1.0, 1.1} V ($i \in$ {1, 2, ..., 11}). The contact resistance $R_{contact}$ was set to 550 Ω in all tests. Red trace: Abscissa $N_{disc}^{(r)}$ of the right crossing between each pair of RESET and SET SDRs from the ReRAM cell DRM of Figure 9 versus the respective label V_m^*. The similar trends of the two datasets provide clear evidence for the power of the system-theoretic DRM analysis method to predict the level, around which the memory state is bound to oscillate at steady-state, upon periodic stimulation of the fading memory ReRAM device.

As shown in Figure 12, the locus of the mean value $\langle N_{\mathrm{disc}}^{(\mathrm{s-s})} \rangle$ of the steady-state oscillatory waveform $N_{\mathrm{disc}}^{(\mathrm{s-s})}$ of the disc oxygen vacancy concentration N_{disc} versus the stimulus peak value $\hat{\nu}_{\mathrm{s}}$, as derived by processing the numerical simulation results from the input amplitude sweep analysis under focus, is closely approximated by the characteristic, obtained by plotting the right crossing $N_{\mathrm{disc}}^{(\mathrm{r})}$ between each of the paired RESET and SET SDRs from Figure 9 versus the associated label V_{m}^{*}.

The numerical investigations, which resulted in the data displayed in Figure 12, reveal how the time average of the asymptotic oscillation in the memory state, upon periodic stimulation of the VCM cell, may be modulated by tuning the input amplitude. Moreover, with reference to Figure 11, as the excitation frequency increases, the DRM-based prediction of the level, around which the disc oxygen vacancy concentration is bound to oscillate, after transients decay to zero, may improve, while, concurrently, the amplitude of this oscillation reduces. This result may inspire the future exploitation of the fading memory of the ReRAM device for implementing a novel scheme to write data into its physical structure. Toward the development of a strategy to leverage fading memory effects to program a desired resistance level into the ReRAM device, numerical investigations were conducted to gain a deeper understanding of the influence of some critical parameter on the steady-state behavior of the periodically-driven VCM cell. **Figure 13**a,b, shows respectively how the frequency of a purely-AC periodic triangular voltage stimulus ν_{s}, let fall across the VCM cell, modulates the amplitude $\widehat{N}_{\mathrm{disc}}^{(\mathrm{s-s})}$ and the mean value $\langle N_{\mathrm{disc}}^{(\mathrm{s-s})} \rangle$ of the steady-state oscillatory waveform $N_{\mathrm{disc}}^{(\mathrm{s-s})}$ of the disc oxygen vacancy concentration, for each input peak value $\hat{\nu}_{\mathrm{s}}$ from the set

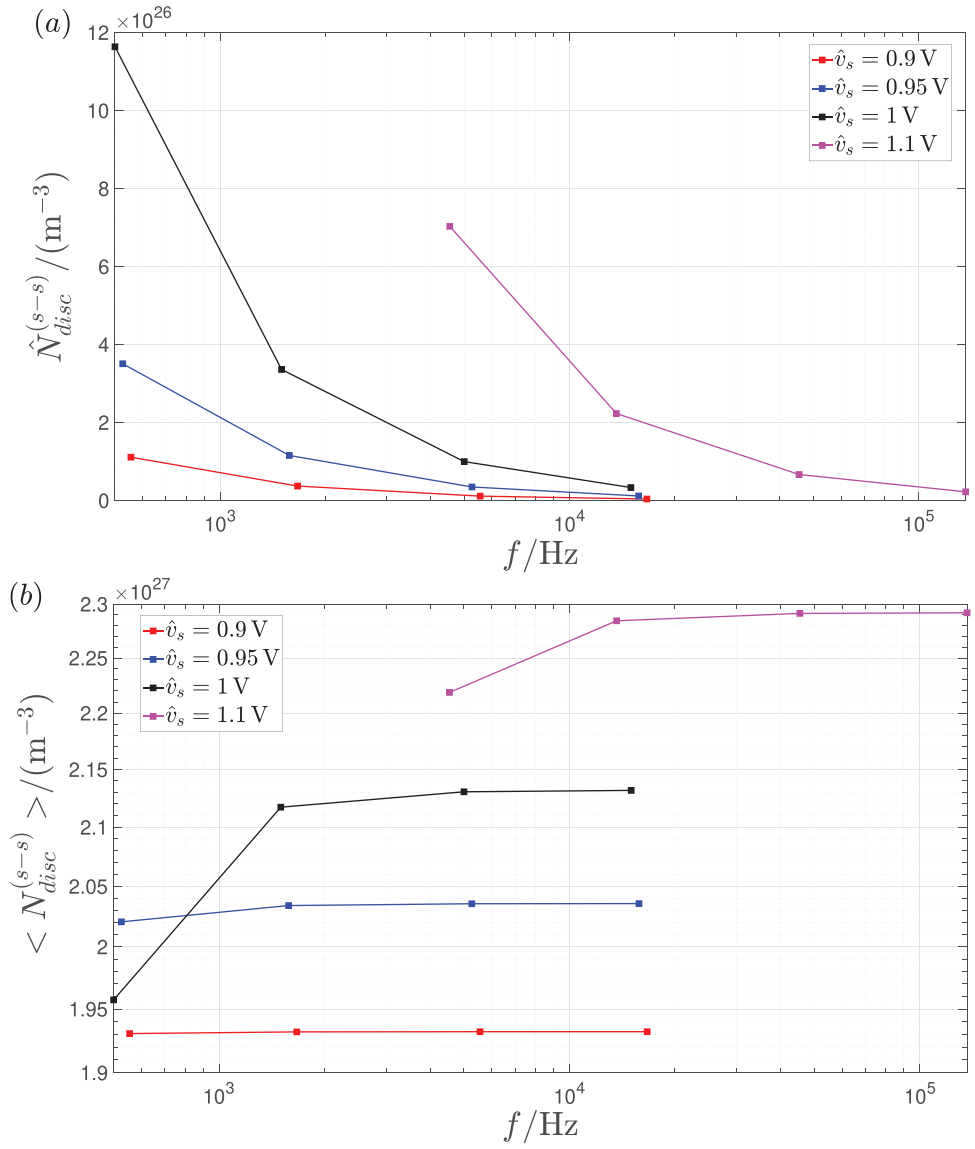


Figure 13. a) Dependence of the amplitude $\widehat{N}_{\mathrm{disc}}^{(\mathrm{s-s})}$ and b) of the mean value $\langle N_{\mathrm{disc}}^{(\mathrm{s-s})} \rangle$ of the steady-state oscillation $N_{\mathrm{disc}}^{(\mathrm{s-s})}$ in the memory state upon the excitation frequency f_{s}, under the application of a purely-AC periodic triangular voltage stimulus ν_{s} across the ReRAM device, for each input peak value $\hat{\nu}_{\mathrm{s}}$ in the list {0.9, 0.95, 1, 1.1} V, and either initial condition $N_{\mathrm{disc,\,0}}$ from the set $\{76 \times 10^{24}, 3 \times 10^{27}\}$ m^{-3}.

{0.9, 0.95, 1, 1.1} V, and either initial condition $N_{\text{disc, 0}}$ in the list $\{76 \times 10^{24}, 3 \times 10^{27}\}$ m^{-3}.

Next, with reference to **Figure 14**, the contact resistance R_{contact}, one of the model parameters, which can be modified over the device fabrication process, is swept across a set of discrete values, namely {0.4, 0.55, 0.75, 1, 1.5, 2} kΩ, to study the influence of its variation on both the existence and location of the left and right crossings between a particular pair of RESET and SET SDRs, respectively associated to a positive and negative DC voltage V_{m} of modulus $V_{\text{m}}^{*} = 1$ V (see plot (a)). The time average $\langle N_{\text{disc}}^{(\text{s-s})} \rangle$ of the oscillation in the disc oxygen vacancy concentration, at the end of the transient phase, as

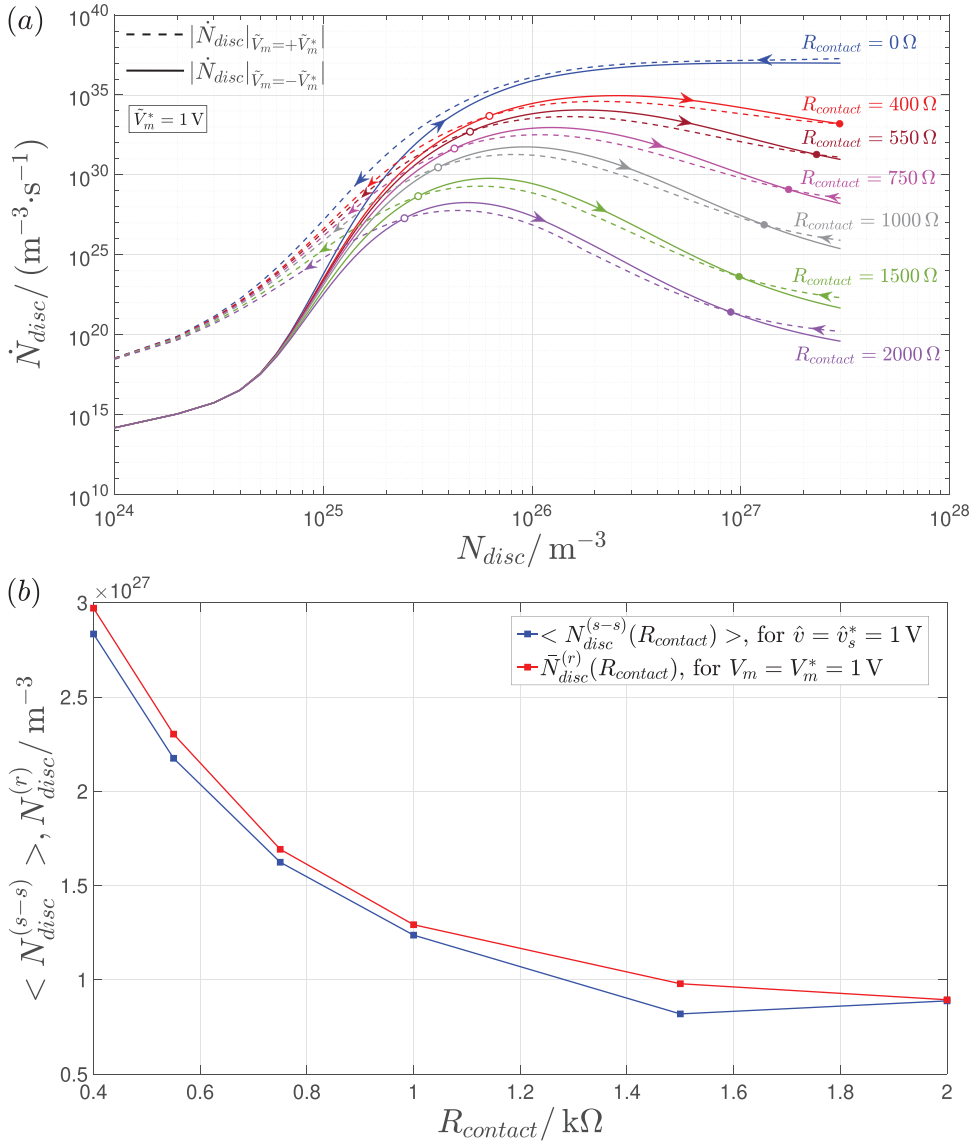


Figure 14. a) Modulation of a pair of RESET (dashed lines) and SET (solid lines) SDRs from the DRM of the VCM cell, namely the one identifiable with the label $V_{\text{m}}^{*} = 1$ V, through a sweep in the contact resistance R_{contact} across the values in the set {0, 0.4, 0.55, 0.75, 1, 1.5, 2} kΩ. Employing some stack engineering strategy, the contact resistance may be potentially tuned to allow the exploitation of the fading memory of the ReRAM cell for application purposes. In the unrealistic case, where the contact resistance is assumed to be null, no intersection appears between the paired SDRs over the memory state existence domain $\mathcal{D}$. b) Qualitative and quantitative agreement between the trend of the locus of the right crossing $N_{\text{disc}}^{(\text{r})}$ of the RESET and SET SDRs, paired through the label $V_{\text{m}}^{*} = 1$ V, versus the contact resistance R_{contact}, as extracted from plot (a) (red trace), and the course of the data, visualizing the dependence of the mean value $\langle N_{\text{disc}}^{(\text{s-s})} \rangle$ of the steady-state oscillatory waveform $N_{\text{disc}}^{(\text{s-s})}$ of the memory state, under the application of a purely-AC periodic triangular voltage stimulus v_{s}, of unitary amplitude $\hat{v}_{\text{s}}$, across the device, upon the contact resistance itself (blue trace). In each numerical simulation, for the derivation of the blue trace, the excitation frequency f_{s} was adapted to the contact resistance value R_{contact}, according to the discussion in Remark 5. The ith value in the set $\{7.5 \times 10^{3}, 1 \times 10^{3}, 7.5 \times 10^{1}, 7.5 \times 10^{-2}, 2.5 \times 10^{-5}, 5 \times 10^{-7}\}$Hz was assigned to the excitation frequency f_{s} in the test, where the contact resistance value R_{contact} was chosen as the ith element from the list {0.4, 0.55, 0.75, 1, 1.5, 2} kΩ ($i \in$ {1, 2, ..., 6}). Each periodic stimulation test was repeated twice, specifically for each initial condition $N_{\text{disc, 0}}$ from the set $\{1 \times 10^{26}, 3 \times 10^{27}\}$ m^{-3}, in order to ascertain the approach of the ReRAM device memory state toward the very same asymptotic solution, from two starting points, lying one below and one above the steady-state oscillatory waveform itself, as resulting from the fading memory of the ReRAM cell.

a purely-AC periodic triangular voltage stimulus v_s, of amplitude $\hat{v}_s = 1$ V and frequency, adapted to the parameter under sweep, according to the specifications reported in Remark 5, is let fall across the ReRAM cell, initially programmed into either of two resistance states, corresponding to a memory state initial condition $N_{disc,\,0}$, chosen from the set $\{1 \times 10^{26}, 3 \times 10^{27}\}$ m^{-3}, is shown as a function of the contact resistance $R_{contact}$ through a blue trace in Figure 14b. The red trace in the same plot shows how well does the right crossing $N_{disc}^{(r)}$ between each pair of RESET and SET SDRs from Figure 14a, except the blue-colored one, approximate the level $\langle N_{disc}^{(s-s)} \rangle$, around which the disc oxygen vacancy concentration is found to oscillate at steady state, in the periodic stimulation test, run after setting the contact resistance to the relevant value. When the contact resistance is assumed to be null, which is an unrealistic scenario, the corresponding pair of RESET and SET SDRs, shown in blue in Figure 14a, never intersect one with the other, over the entire memory state existence domain $\mathcal{D}$. In this case, irrespective of the initial condition, the stimulation of the ReRAM cell with a purely-AC periodic triangular voltage stimulus v_s, of amplitude $\hat{v}_s = 1$ V, and frequency $f_s = 7.5 \times 10^7$ Hz, results in a progressive decrease in the memory state, which, after transients vanish, is found to revolve cyclically around a tiny oscillation, clipped at the lower bound $N_{disc,\,off}$ in its existence domain $\mathcal{D}$. This reveals the crucial role, that the contact resistance plays in the emergence of an oscillatory steady state, unaffected by boundary effects, for the disc oxygen vacancy concentration.[31]

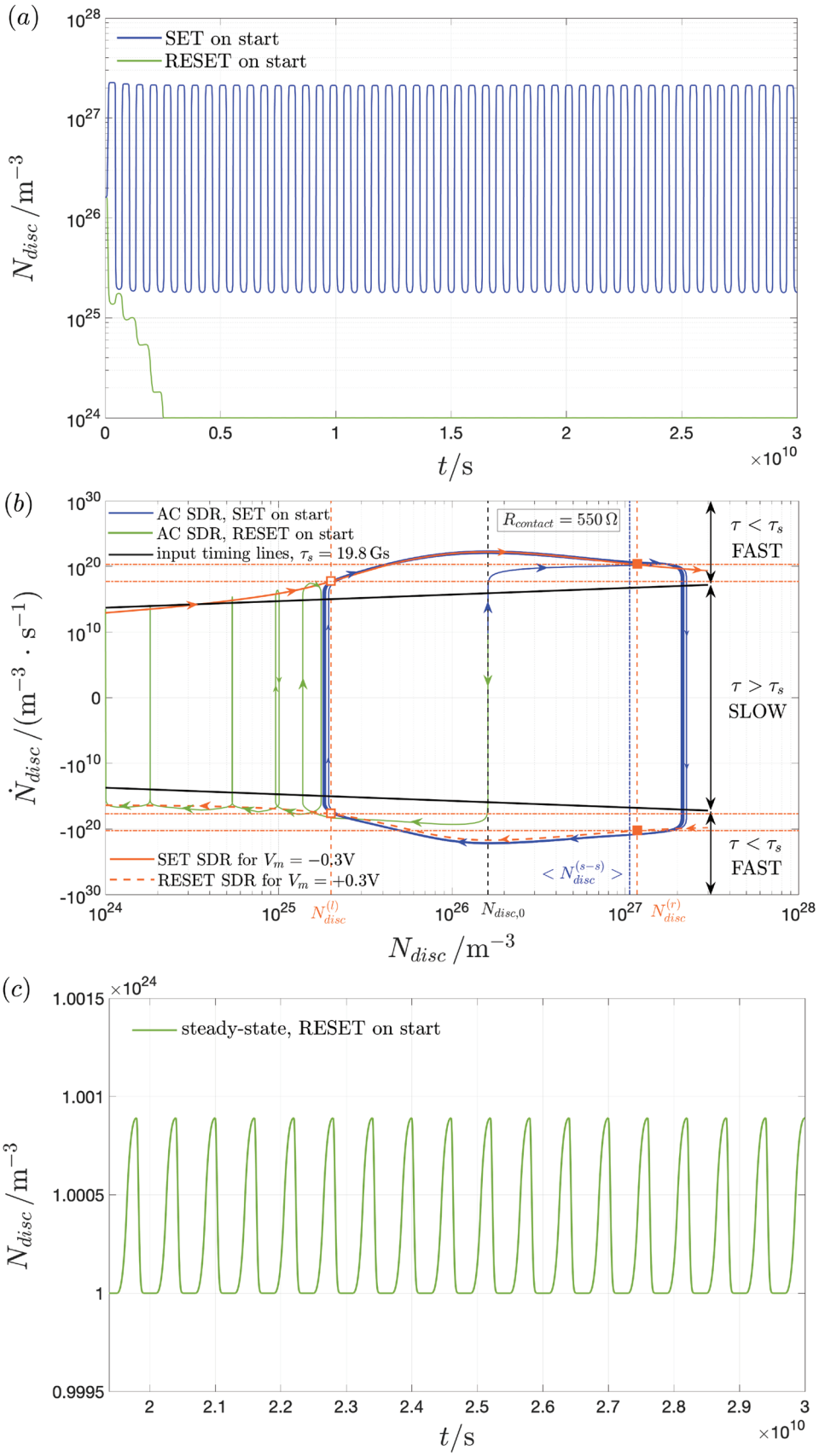
5.3. Signs of Local Fading Memory: Bistability in the Periodically-Forced ReRAM Cell

Local fading memory[56,57] refers to a local form of fading memory. In particular, a forced system is said to have local fading memory under a given input, if the space, spanned by its state variables, may be decomposed in two or more regions, within each of which the stimulus drives any possible trajectory toward a distinct attractor. In each of these state-space regions, and thus locally, the stimulus erases the memory of the system, which is bound to converge asymptotically toward the relevant attractor, irrespective of the initial condition. Section S2, Supporting Information, provides further details on the concept of local fading memory. For the periodically-driven memristor under focus in this study, the steady-state branch of an AC SDR in the dN_{disc}/dt versus N_{disc} plane[58] may be interpreted as a possible attractor for the associated JART VCM v1 DAE sets (1)–(2).

Extensive numerical investigations, based upon this model, have very recently unveiled that, at least in principle, the *AC fading memory of the periodically-driven ReRAM device has a local nature*. As will be revealed shortly, however, the experimental observation of input-induced multi-stability in the physical stack may require an unreasonably-long time frame, which prevents its exploitation for application purposes, at least in regard to the VCM cell under focus in this manuscript (see below for more details). Focusing now on the model simulation-based findings, the numerical integration of the DAE set (1)–(2), under properly-calibrated input settings, reveals that the VCM cell may exhibit bistability. Specifically, after transients decay to zero, it may exhibit one of two possible oscillatory behaviors, depending upon the initial resistance, programmed into its physical stack, when a particular purely-AC periodic voltage stimulus is let to drop between its terminals. Interestingly, this shows that the initial condition $N_{disc,\,0}$ may play an important role on the asymptotic dynamics of the periodically-forced ReRAM device. Inspecting the DRM of Figure 9, it is clear that, for each RESET and SET SDR pair, the RESET forces are way stronger than the SET forces in the high resistance regime. In fact, this explains why, if the same periodic stimulus v_s of Figure 8b were applied across the VCM cell, in a scenario, where the latter were preliminarily initialized in a very high resistance state, the RESET forces would prevail over the SET ones over each input cycle, during the transient phase, and, asymptotically, similarly as in the investigation carried out earlier for $\hat{v}_s = 1$ V, $f_s = 7.5 \times 10^7$ Hz, and $R_{contact} = 0\ \Omega$, the memory state would be found to evolve along a tiny oscillatory waveform, which is clipped at the lower bound $N_{disc,\,off}$ of its existence domain $\mathcal{D}$. Indeed, in general, *according to the predictions of the JART VCM v1 model, the VCM cell has* local fading memory[56] under purely-AC periodic voltage stimuli, exhibiting a steady-state *bistable behavior*[57] in response to any input of this kind.

In order to provide clear evidence for the local fading memory of the periodically-driven ReRAM cell, two numerical simulations of the JART VCM v1 model were set up in such a way that, initializing the disc oxygen vacancy concentration at a fixed value $N_{disc,\,0}$, specifically 1.61×10^{26} m^{-3}, a purely-AC periodic triangular voltage stimulus v_s, of amplitude $\hat{v}_{hat} = 0.3$ V, a sweep rate SR of 6.062×10^{-11} V s^{-1}, equivalent to a frequency $f_s = SR/(4 \times \hat{v}_s)$ of 5.05×10^{-11} Hz, and two phase values, differing by 180° one from the other, fell across its terminals. Setting these input phase values, in such a way that the excitation signal would undergo a positive (negative) excursion over the first half cycle, allows to induce a RESET (SET) transition in the VCM cell over this very same time interval.

This is sufficient to observe a progressive gradual decrease (fast increase) in the memory state, as determined by the predominance of the RESET (SET) forces over the SET (RESET) ones over each cycle in the transient phase, with the ultimate convergence of the disc oxygen vacancy concentration toward a relatively-large (relatively-small) oscillatory solution, revolving around a mean value $\langle N_{disc}^{(s-s)} \rangle$ of 1.06×10^{27} m^{-3} (clipped at the lower bound $N_{disc,\,off}$ in its existence domain $\mathcal{D}$). The mean value $\langle N_{disc}^{(s-s)} \rangle$ of 1.06×10^{27} m^{-3} is approximated rather well by the right crossing point $N_{disc}^{(r)} = 1.17 \times 10^{27}$ m^{-3} between the RESET and SET SDRs, paired through the label $V_m^* = 0.3$ V. With reference to **Figure 15**, whose caption is reported separately at the bottom of page 28, the time waveform of the oscillatory solution, emerging when the input signal assumes positive (negative) values over the first half cycle, is shown as a green (blue) trace in Figure 15a. The green (blue) AC SDR in Figure 15b shows the locus of the time derivative of the memory state versus the memory state itself, as extracted from the numerical simulation data in the first (latter) case. Importantly, with reference to the green trace from Figure 15b, the initial positive excursion of the excitation signal v_s drives the trajectory point $P = (N_{disc}, dN_{disc}/dt)$ to the left of the left crossing point $N_{disc}^{(l)} = 2 \times 10^{25}$ m^{-3} between the corresponding



pair of RESET and SET SDRs, identifiable with the label $V_m^* = 0.3$ V, specifically to the location with abscissa $N_{disc} = 1.37 \times 10^{25}$ m^{-3}, over the first half cycle. Due to the relatively weak SET forces for the range of input values, defined as $[-\hat{v}_s, 0\,V)$, with $\hat{v}_s = 0.3$ V, over the region of the memory state domain $\mathcal{D}$, lying directly to the right of the value attained by N_{disc} at the end of the first half cycle, the subsequent first SET transition of the ReRAM cell is unable to move the trajectory point P back to the right of the left intersection $N_{disc}^{(l)}$ (in fact, the abscissa N_{disc} of P increases only up to 1.76×10^{25} m^{-3}).

As a result, cycle after cycle, the RESET forces prevail over the SET ones, and, inevitably, the memory state is found to revolve along an oscillatory solution, clipped to the lower bound $N_{disc,\,off}$ in its existence domain $\mathcal{D}$, after transients vanish. Figure 15c provides a zoom-in view of the steady-state part of the oscillatory solution of the state Equation (1), in this scenario, where the device undergoes a RESET transition over the first input half cycle. While strictly speaking, the local form of the AC fading memory of the ReRAM device should be investigated by fixing the stimulus settings, while varying the initial condition, the simulation pair, resulting in the data visualized in Figure 15, may be employed for such a testing purpose as well. In fact, discarding the data extracted during the first input half cycle from the green trace, the time waveform of the "new" signal may be interpreted as the solution of the state equation under the same input as the one, which prompted the emergence of the blue trace, but for a different initial condition, namely $N_{disc,\,0} = 1.37 \times 10^{25}$ m^{-3}. In fact, it may be concluded that, in the scenario, where the input settings are fixed, such that the purely-AC periodic triangular voltage stimulus of amplitude $\hat{v}_s = 0.3$ V and frequency $f_s = 5.05 \times 10^{-11}$ Hz is let undergo a negative excursion over the first half cycle, the initial condition $N_{disc,\,0} = 1.61 \times 10^{26}$ m^{-3} ($N_{disc,\,0} = 1.37 \times 10^{25}$ m^{-3}) sits in the basin of attraction of the first (second) steady-state attractor, lying entirely within (clipped at the lower bound of) the memory state existence domain $\mathcal{D}$. Here, the threshold value $N_{disc,\,th}$, representing the *separatrix*[58] between the basins of attraction of the two attractors, is found to lie between 1.37×10^{25} and 1.94×10^{25} m^{-3}, where the latter value denotes the disc oxygen vacancy concentration at the end of the first input cycle for $N_{disc,\,0} = 1.61 \times 10^{26}$ m^{-3}. The observations from Figure 15 clearly reveal the local AC fading memory of the periodically-driven VCM cell, according to the strict system-theoretic definition, reported above.

Whether this very interesting bistable behavior, unveiled via a system-theoretic investigation of the memristor model, will ever be observed in a practical experiment, is an open issue. First of all, while, according to the JART VCM v1 model, the lower and upper bound in the memristor state existence domain have physical grounds, they purely define limits of validity for the underlying mathematical description. Second, as briefly mentioned in the above hint, in order to trigger the emergence of a steady state, resulting from local fading memory phenomena, from either of two different initial conditions, sitting on distinct basins of attraction, within a few input cycles, the amplitude $\hat{v}_s$ of the excitation signal, for the simulation pair, which resulted in the data visualized in Figure 15, was set to a very low value, and, concurrently, an experimentally-irrelevant tiny number, in line with Remark 5, was assigned to the frequency f_s of the stimulus itself. Increasing the input peak value $\hat{v}_s$, and adapting the excitation frequency f_s to an experimentally-doable value, accordingly, while keeping the initial condition $N_{disc,\,0}$ fixed to the same value as in Figure 15, namely 1.61×10^{26} m^{-3}, the memory state solution N_{disc}, referring to the scenario, where the input v_s undergoes a positive transition over the first half cycle, would take an unreasonably-long number of periods to approach the oscillation, clipped at $N_{disc,\,off}$, since here $|dN_{disc}/dt|$ reduces progressively across a huge number of decades over consecutive input cycles.

As a concluding remark, while a particular mathematical model, whose accuracy in reproducing the highly-nonlinear dynamics of ReRAM cells was demonstrated in previous works,[36] has been employed in this paper to gain a deep understanding of the mechanisms, underlying resistance switching transitions in memory devices of this kind under both DC and purely-AC periodic inputs, allowing to infer under which conditions may they lose memory upon stimulation, which may inspire the implementation of novel mem-computing paradigms,[59] in the years to come, it is instructive to point out that also the past history of other physical memristor realizations may be erased via appropriate excitation, as recently revealed in ref. [32]. However, very importantly, the powerful circuit-

Figure 15. a) Time course of the disc oxygen vacancy concentration from a fixed initial condition, particularly $N_{disc,\,0} = 1.61 \times 10^{26}$ m^{-3}, under the application of a purely-AC periodic triangular voltage stimulus v_s, of amplitude $\hat{v}_s = 0.3$ V, frequency $f_s = 5.05 \times 10^{-11}$ Hz, and either of two phases, differing by 180°, across the ReRAM cell. When the excitation signal undergoes a negative (positive) excursion over the first half period, a SET (a RESET) transition emerges in the VCM device, as may be inferred by inspecting the blue (green) memory state versus time locus. b) AC SDR resulting from the solution to the state Equation (1), in the scenario, where the input signal assumes negative (blue trace) or positive (green trace) values in the first half cycle. Irrespective of the simulation scenario, as expected from the theoretical analysis from Section 5.2, when the trajectory point $P = (N_{disc}, dN_{disc}/dt)$ travels across the region, enclosed between the black solid negative and positive input timing lines, the device dynamics would appear slow, to the eyes of an external observer. On the other hand, when the trajectory point visits the region below (above) the positive (negative) input timing line, an experimenter would appreciate fast dynamics in the RESET (SET) transition of the VCM cell. In regard to the blue trace, the mean value $\left\langle N_{disc}^{(s-s)} \right\rangle = 1.06 \times 10^{27}$ m^{-3} of the oscillatory signal $N_{disc}^{(s-s)}$, which shows the time evolution of the disc oxygen vacancy concentration at steady state, for the scenario, where the input undergoes a SET transition over the first half cycle, is found to be approximated rather well by the right crossing $N_{disc}^{(r)} = 1.17 \times 10^{27}$ m^{-3} between the orange dashed RESET and solid SET SDRs from the DRM of Figure 9, referring to the assumption that a positive and negative DC voltage V_m, of modulus V_m^* equal to the amplitude $\hat{v}_s$ of the excitation signal v_s, falls across the physical stack, respectively. It is important to observe that the orange hollow (filled) square on the left (right) crossing between the RESET and SET SDRs, identifiable through the label $V_m^* = 0.3$ V, from the ReRAM cell DRM of Figure 9, is duplicated in plot (b), where the polarity of the switching speed is accounted for, along the vertical axis, resulting in the appearance of two markers of the same kind at fixed abscissa but oppositely-signed ordinates. c) Zoom-in view of the time waveform of the oscillatory solution to the state Equation (1), as observed in the scenario, where the first half cycle of the stimulus induces a RESET transition in the VCM cell. In both simulations $R_{contact}$ was set to 550 Ω.

and system-theoretic concepts, adopted in this work to predict complex nonlinear phenomena in a representative ReRAM cell, may be applied mutatis mutandis to analyze the switching dynamics of different memory devices in the near future. Furthermore, the insights, drawn from the system-theoretic investigations, reported in this manuscript, allow to set up ad hoc constraints for appropriate device modeling, such as

1) The requirement to formulate the state equation in such a way to provide, for both the SET and RESET processes, an ensemble of non-monotonic SDRs with concave- down shape, of the kind illustrated in Figure 9, in case, as it is frequently observed in ReRAM cells, resistance switching transitions are characterized by an early abrupt phase, while experiencing a significant deceleration, subsequently.
2) The need to express the state equation in such a way that each RESET SDR, corresponding to a given positive DC voltage $V_m = V_m^*$, let fall across the device, may feature a flatter region, around the respective hump, as compared to the SET SDR, associated to a DC negative voltage $V_m = -V_m^*$, applied between the device terminals, so as to capture the asymmetry between the on and off switching dynamics, and, particularly, the narrower range of variation for the ReRAM cell resistance over a RESET transition as compared to what is the case over the corresponding SET transition.
3) The necessity to write down the state equation in such a way that, correspondingly, any two SET and RESET SDRs, associated to a given memristor bias voltage modulus, admit a specific crossing, to the left (right) of which, locally, the SET (RESET) forces dominate over the RESET (SET) ones, as illustrated in Figure 9, provided, as it is typically the case in ReRAM cells, due to input-induced memory loss effects, the application of a purely-AC periodic stimulus, of amplitude equal to the aforementioned memristor voltage modulus, across the device, drives the disc oxygen vacancy concentration toward an asymptotic solution, oscillating around a level, which lies within the bounds of the memory state existence domain, signaling a perfect balance between the effects of the counteractive SET and RESET forces on the device dynamics over each input cycle.

6. Conclusions

This work provides a unique example of the benefits, which a cooperative research between theoreticians and experimentalists may provide to the scientific community, devoting efforts to explore the full potential of ReRAM devices for future electronics. In this paper, a powerful system-theoretic tool, known as DRM, is employed to gain a deep understanding of the mechanisms, underlying the resistance switching phenomena, which emerge in a TaO_x-based ReRAM device, fabricated at the Peter Grünberg Institut 7 (PGI-7) in the Forschungszentrum Jülich (FZJ), under both DC and purely-AC periodic stimulation. The most significant results of this comprehensive study, combining experimental and theoretical analyses, are listed below:

1) Experimental evidence for the DC fading memory of the ReRAM cell, that is, for the emergence of history erase effects, induced via DC RESET (SET) stress, in its physical stack, found to exhibit a unique asymptotic behavior, sitting on its highest (lowest) possible resistance state, as a result, as well as for the coexistence between DC fading memory and non-volatility, was provided.
2) As an insightful information, employable as a constraint in the future development of predictive models of other similar ReRAM devices, the DRM analysis has revealed how necessary is the existence of a hump on any RESET (SET) SDR for reproducing the typical time course of the current in response to a DC positive (negative) voltage stimulus, which reflects the progressive transition of the VCM cell, initially programmed into a relative low (high) resistance state, through two gradual phases, separated by an abrupt one.
3) While a rigorous measure for the abrupt regime in the ReRAM cell response to a positive (negative) DC pulse stimulus was provided, the system-theoretic analysis showed how, actually, it is the ratio between the time duration of this phase and the time, elapsed between the time of application of the pulse stimulus, and the time, at which the sharp RESET (SET) transition begins, which crucially determines whether, to the eyes of an experimenter, the RESET (SET) switching process appears fast or slow.
4) A new graphic tool, called current DRM (C-DRM), representing a current-based variant of the DRM, has been introduced to enable the system-theoretic analysis of data, measurable in lab tests on device samples.
5) Experimental proof for the AC fading memory of the ReRAM cell, that is, for the emergence of history erase effects, induced via purely-AC periodic stimulation, in its physical stack, found to exhibit a unique asymptotic oscillatory behavior, as a result, was provided (see Section S5, Supporting Information, for a proof of evidence of the coexistence between AC fading memory and non-volatility in the ReRAM cell).
6) Augmenting the information available on the ReRAM cell DRM, with two timing diagrams, one associated to the fixed time scale of a periodic stimulus, and one to the time-dependent time scale of the associated memristor response, the system-theoretic investigation revealed how, at any given time, it is the ratio between these two time scales, which crucially determines whether, in a practical experiment, the device RESET (SET) transition, over the positive (negative) excursion of the excitation signal, in each cycle, would be appreciated slow or fast, and how slow or fast it would appear, to an external observer.
7) The capability of the DRM tool to predict the mean value of the steady-state oscillation in the disc oxygen vacancy concentration, under purely-AC periodic stimulation of the device, especially for excitation frequencies so high to induce a noticeable memory state decrease (increase), over the positive (negative) input excursion phase in each cycle, only when the excitation voltage approaches its absolute maximum (minimum) value, was demonstrated.
8) As a follow-up from the previous remark, when, under suitable periodic excitation of the device, its resistance is found to oscillate, asymptotically, around a level, within the allowable operating domain, then the pair of RESET and SET SDRs, extracted from the cell DRM for the maximum and minimum values of the voltage stimulus, respectively, necessarily cross in a point, to the left (right) of which the SET

(RESET) dynamics are stronger than the RESET (SET) ones, which may be used as an additional constraint in the development of predictive models of similar ReRAM devices.

9) Signs for the appearance of local fading memory phenomena in the periodically-driven ReRAM device were recently uncovered via extensive numerical investigations, which revealed how, in general, under a given purely-AC periodic voltage stimulus, the VCM cell may exhibit one of two distinct oscillatory behaviors, after transients vanish, depending upon the choice of the initial condition.

10) In view of a future exploitation of the fading memory of the ReRAM cell for electronics applications, it is worth pinpointing that the amplitude of the oscillatory response of the periodically-driven device reduces with the input frequency, while its mean value may be modulated through the stimulus strength across a certain range, which can be potentially optimized in the future through stack engineering, as revealed in this paper through the investigation of the effects of the contact resistance on the shape of the RESET and SET SDRs associated to a given V_m^* value, and, ultimately, on the location of their right crossing, which predicts the level around which the memory state is bound to oscillate under a purely-AC periodic triangular voltage stimulus of amplitude $\hat{v}_s = V_m^*$.

7. Experimental Section

ReRAM Device Fabrication: For the TaO_x ReRAM device fabrication, a 5 nm-thick titanium (Ti) layer and a 30 nm-thick platinum (Pt) layer were first laid down one after the other by physical vapor deposition (PVD) on a thermally-grown 430 nm-thick silicon dioxide (SiO_2) layer sitting on a silicon (Si) substrate. After patterning the Pt bottom active electrode (AE), a 7 nm-thick sub-stoichiometric tantalum oxide (TaO_x) layer was deposited by reactive sputtering under a flow of argon (Ar) and oxygen (O_2), composing the 77% and 23% of the gaseous mixture, respectively, and delivering power at radio frequencies. These steps lead to the Pt (25 nm)/Ta (15 nm)/TaO_x (7nm)/Pt (30 nm) ReRAM device sketched in Figure 1a. Further details on the device fabrication can be found in ref. [35]. The electrical characterization of devices of this kind was performed at room temperature using a custom-designed measurement setup.[34]

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

dynamic route maps, fading memory, memristive devices, redox-based random access memories, valence change memories

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